Summer school on Epitaxy
MATEPI 2025
Porquerolles June 22-27 2025

Integration of Epitaxial Systems for Electronics Applications

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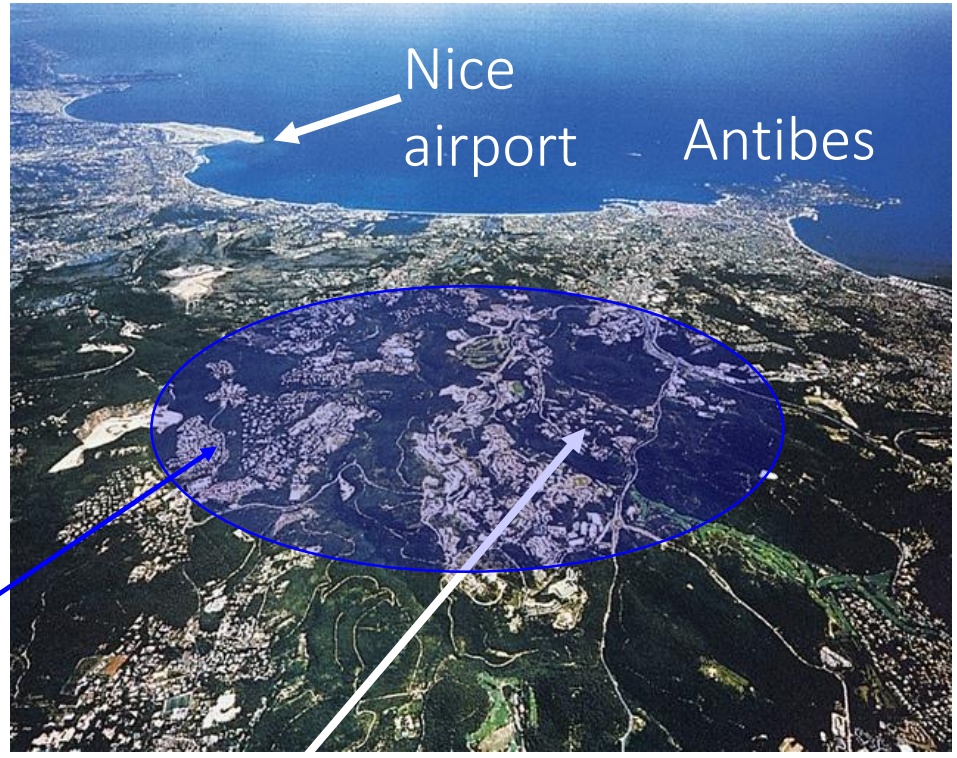


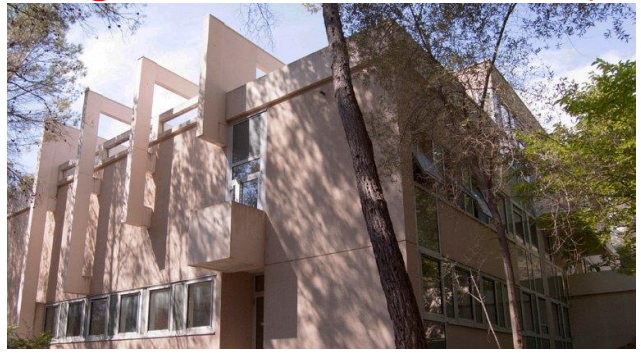
Sophia Antipolis: 30 000 jobs

1200 companies / labs

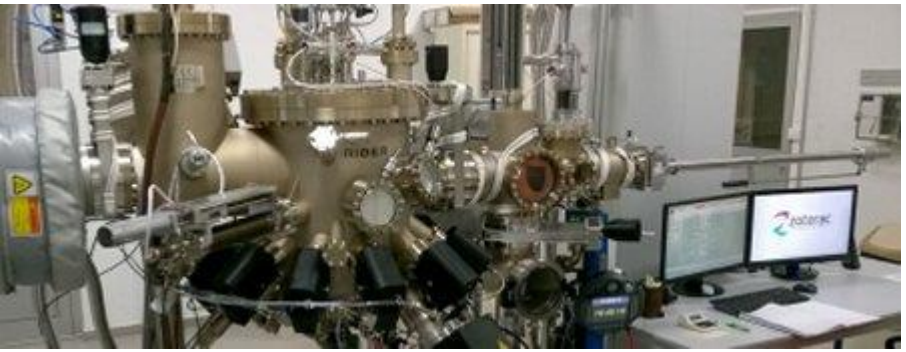
- Research Labs (academic & private)
- Companies (medical, software, electronic, numerical related to telecoms…)

CRHEA: Research Center for Hetero-Epitaxy & Applications

(~ 70 pers., researchers, professors, students, engineers, administratives)



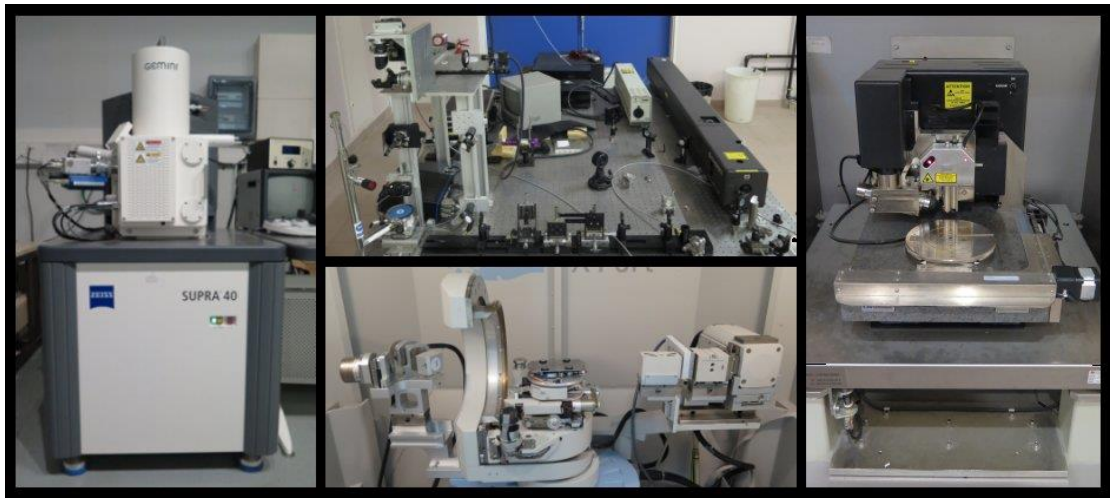
Activities



EPITAXY

Semiconductors

(MBE, MOCVD)



Optical Char.

PL, µ-PL, CL

Electrical Char.

(I-V, Hall, C-V)

Clean Room Devices

(LEDs, HEMTs)

Structural Characterization

(XRD, AFM, SEM, TEM)

- **GaN : LEDs, µ-cavities, µ-lasers, electronics (RF, power)**
- **ZnO : IR, THz (QWIP, QCL), µ-cavities (polaritons)**
- **SiC : power electronics, buffer for GaN, MEMS**
- **Graphene & 2D materials (MoS_2 , WS_2 …): CVD growth, VdW epitaxy**
- **Metasurfaces –**
- **Nano-photonics, quantum technologies –**

} **micro- / nano-fabrication on nitrides, oxides, SCs**

Outline

- **Si Electronics**
  - Si-based Technology: Field Effect Transistor, Metal-Oxide FET & CMOS Technology
  - From MOSFET to Integrated Circuits
  - Scaling: motivations, issues & solutions (technological/material integration)
- **Heterogeneous Integration**
  - Heterogeneous Material Integration on Si Platforms
  - From MOSFET to HEMT
- **SiGe & III-V Technology**
  - Strained Si MOSFET
  - SiGe channels & III-V HEMTs
  - Epitaxy Defect Engineering, Nanowires
- **Nitrides semiconductors & 2D Materials**
  - Nitride Materials – AlGaN/GaN HEMTs
  - 2D Materials
- **Conclusions & perspectives**

Si Electronics

Si-based technology

Why Si ?

Silicon: abundant (2nd element (28%) after oxygen (46%)), cheap and simple purification process:
Reduction:
Silicon dioxide (SiO_2) is reduced (@ 1500-2000 °C) : **$SiO_2 + C \rightarrow Si + CO_2$**

→ Si is metallurgical grade silicon (MG-Si) 98-99% pure.

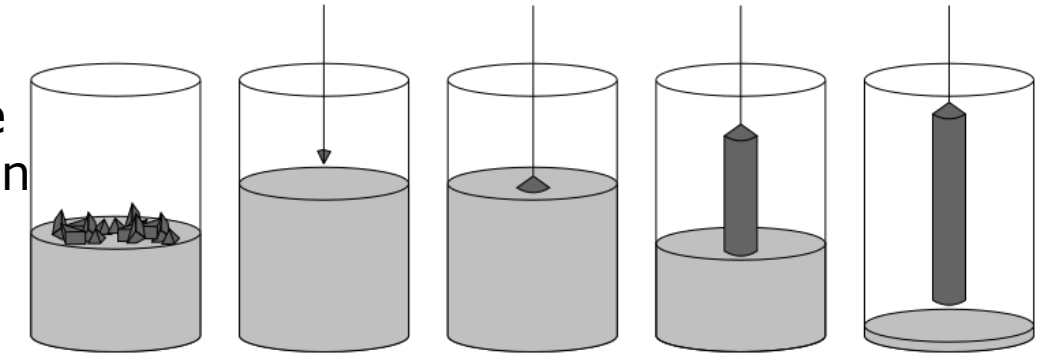
Presence of transition metals --> deep levels in the bandgap with high recombination activity --> unsuitable for use in electronics

Purification in 2 steps:

- MG-Si is reacted with anhydrous HCl (@ 300 °C) to form $SiHCl_3$: **$Si + 3HCl \rightarrow SiHCl_3 + H_2$**
- $SiHCl_3$ is reacted with hydrogen (@ 1100°C) to produce a very pure Si : **$SiHCl_3 + H_2 \rightarrow Si + 3\ HCl$**

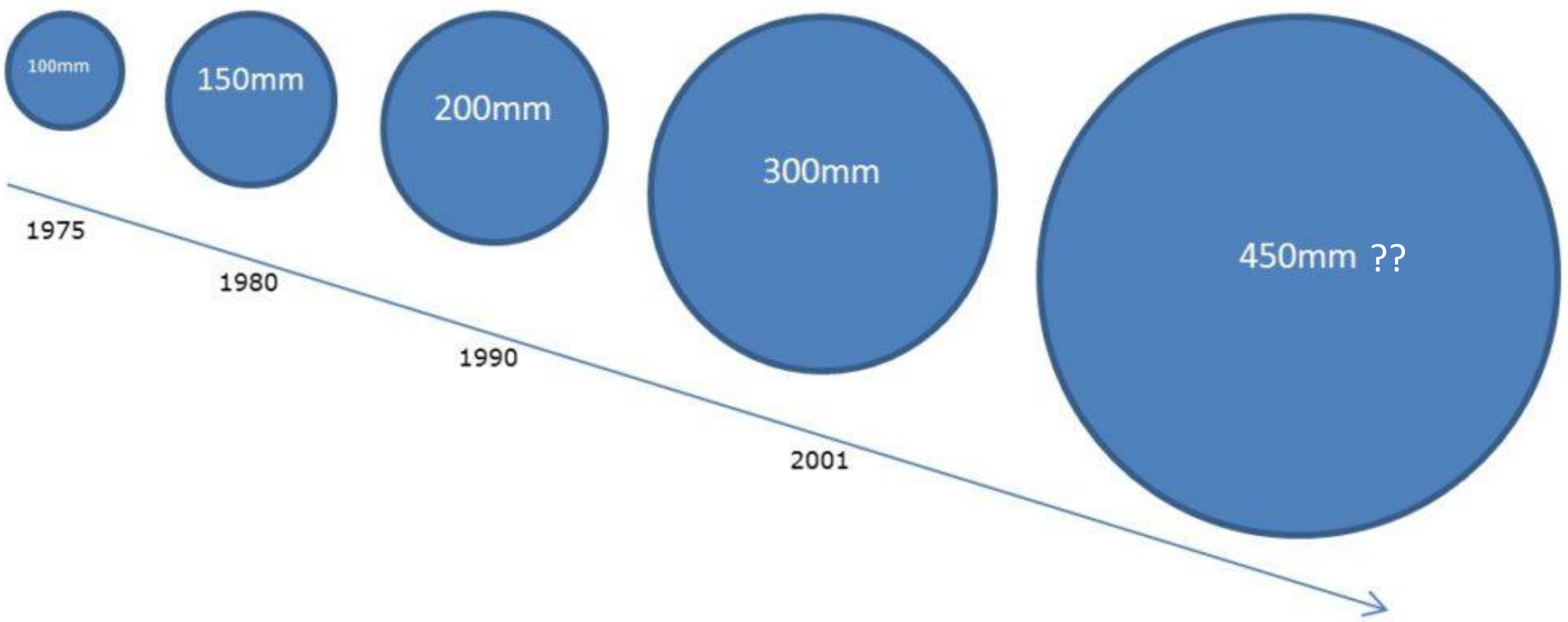
  Reaction inside large vacuum chambers & the Si is deposited onto thin polysilicon rods to produce high-purity polysilicon rods.
  The resulting rods of semiconductor grade silicon are broken up to form the feedstock for the crystallisation process.

- Czochralski (CZ) process (Crystal pulling)
- Floating zone (FZ) process



Si wafers

- **Strong increase of the wafer diameter since the 1960's**
  → **from 100mm to 300 mm**
  --> reduction of the price per transistor & performances improvement



Field Effect Transistor

- **A transistor** is a semiconductor device used to **amplify or switch electronic signals & electrical power**
- **A field effect transistor (FET) uses an electric field to control the flow of current & only one kind of charge carrier**
  - **Amplifier** = electronic device that can increase the power of a signal
  - **Switch** = electrical component that can disconnect or connect the conducting path in an electrical circuit

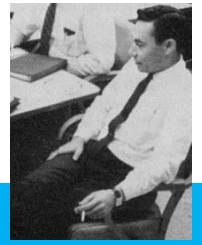
« concept of a field-effect transistor »
Julius Edgar Lilienfeld
(1882 – 1963)

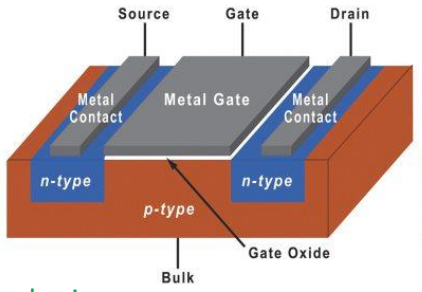
First working device in 1947 by John Bardeen, Walter Brattain and William Shockley (Bell Labs)

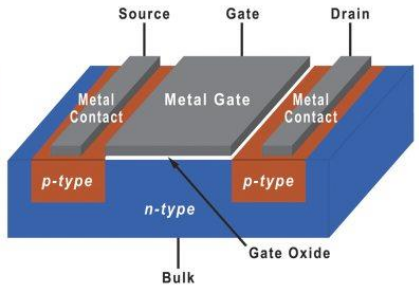
Nobel Prize in Physics in 1956

- **Main type of transistor used = metal–oxide semiconductor field-effect transistor (MOSFET)**

invented by Mohamed Atalla and Dawon Kahng (1959, Bell Labs)







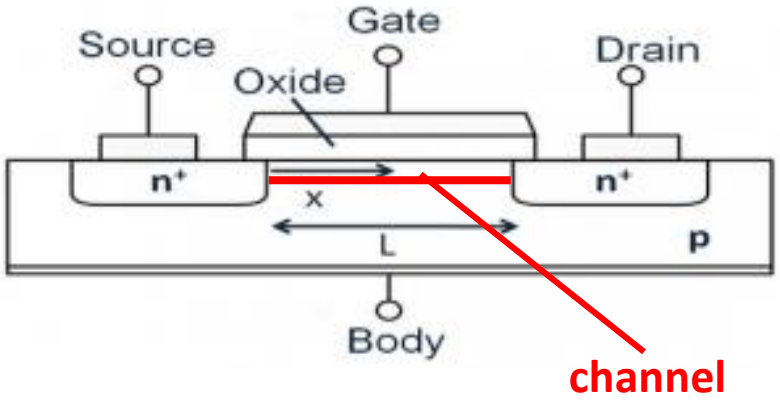
https://www.mksinst.com/n/mosfet-physics

Metal–Oxide semiconductor FET (MOSFET)

- Basic MOSFET devices: Poly-Si as the gate material, SiO_2 as insulator (gate oxide) and Si as substrate.

  → The gate switches on and off the transistor when a voltage is applied, creating an electric field (crossing the gate oxide) that changes the width of the channel region

https://www.elprocus.com/the-fabrication-process-of-cmos-transistor/



- **3 terminal device :**

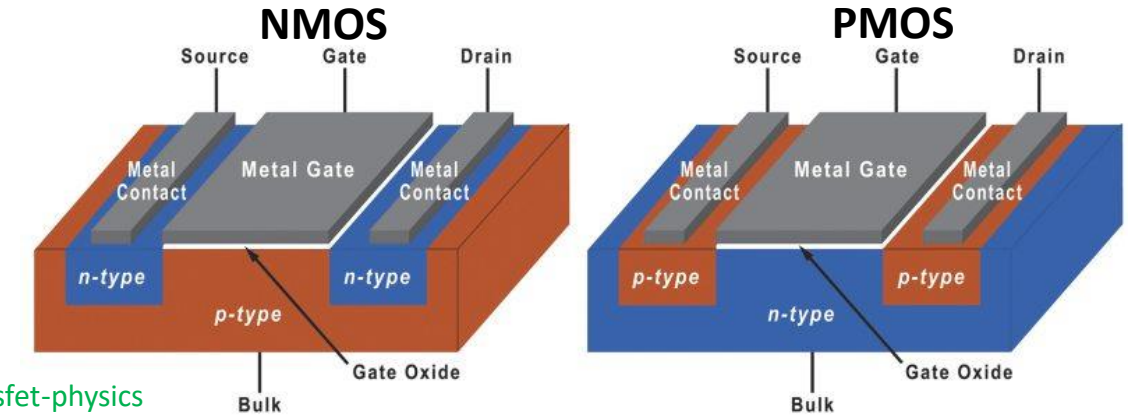
  The Source, Gate, Drain and Body (bulk) are terminals.
  The body is in connection with the source terminal thus forming a three-terminal device such as a field-effect transistor.

- **The functionality of MOSFET depends on the electrical variations in the channel width along with the flow of carriers** (h+ or e-).

  The charge carriers enter into the channel through the source and exit via the drain.

- **The N-Channel MOSFET** has an **N-channel region**

- **The P- channel MOSFET** has a **P- Channel region**



https://www.mksinst.com/n/mosfet-physics

Metal–Oxide semiconductor FET (MOSFET)

- **MOS Transistor main elements & 12-steps fabrication process:**

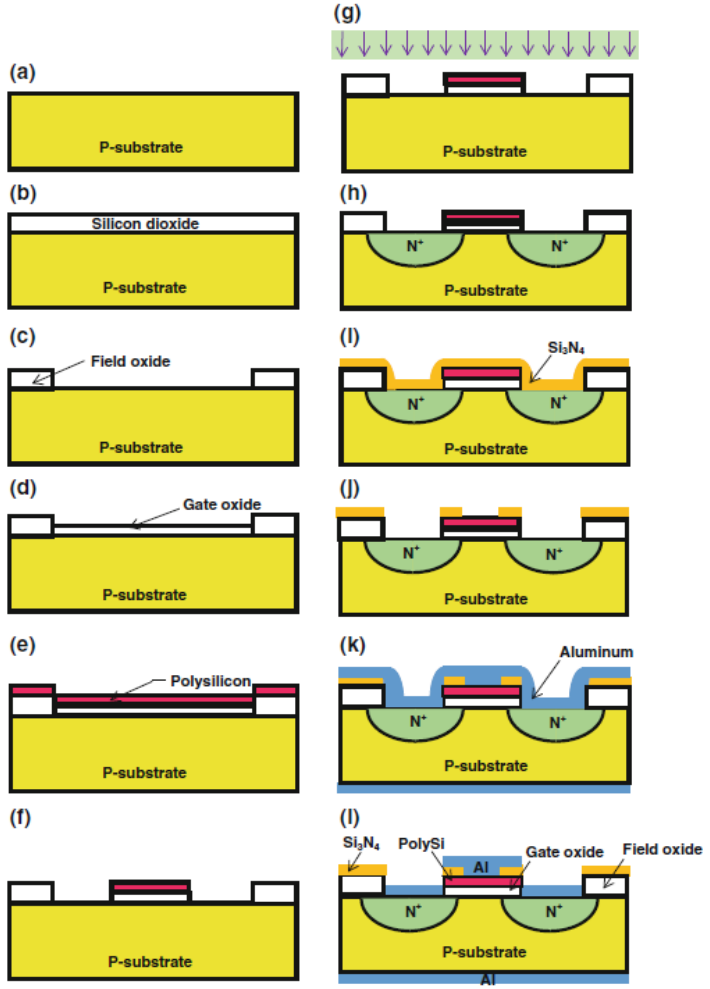
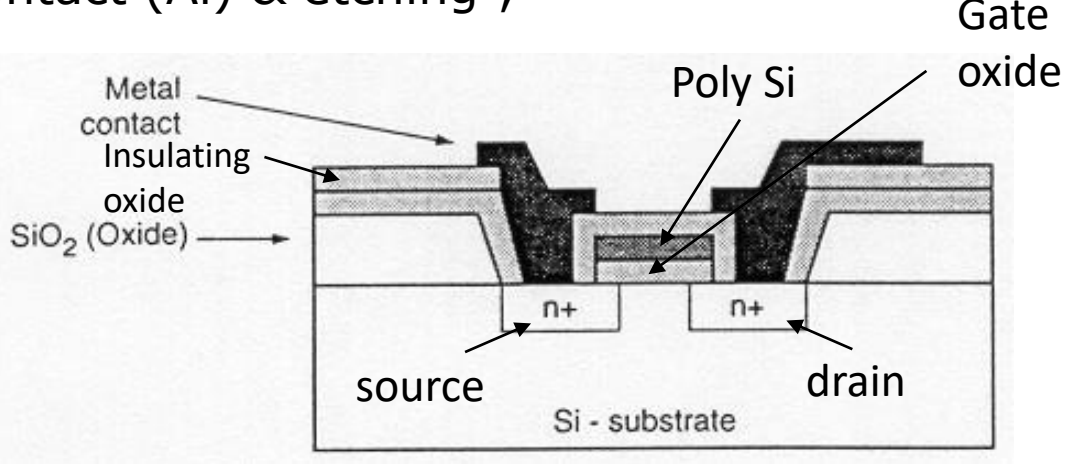


Fig. 4.3 Simple self-aligned polysilicon gate process for N-channel MOSFET fabrication in which polysilicon gate acts as a mask for source/drain formation. Lightly doped source/drain structure formation is excluded. **a** Starting silicon wafer. **b** Field oxidation. **c** Oxide etching. **d** Gate oxidation. **e** Polysilicon deposition. **f** Polysilicon and oxide etching. **g** Source/Drain implant. **h** High temperature annealing. **i** Silicon nitride deposition. **j** Nitride etching. **k** Metal deposition. **l** Metal etching

1. oxidation of the Si substrate (field oxide) + etching part of the SiO_2 ;
2. formation of a thin oxide layer (gate oxide– thermal oxidation) + **deposition of poly Si (by CVD)**;
3. etching + doping (implantation) of Si → creation of the source & drain junctions (self-aligned proc.);
4. **insulating layer of SiO_2 or Si_3N_4 (by CVD)** + etching (contact windows for source & drain) ;
5. deposition of the metal contact (Al) & etching ;

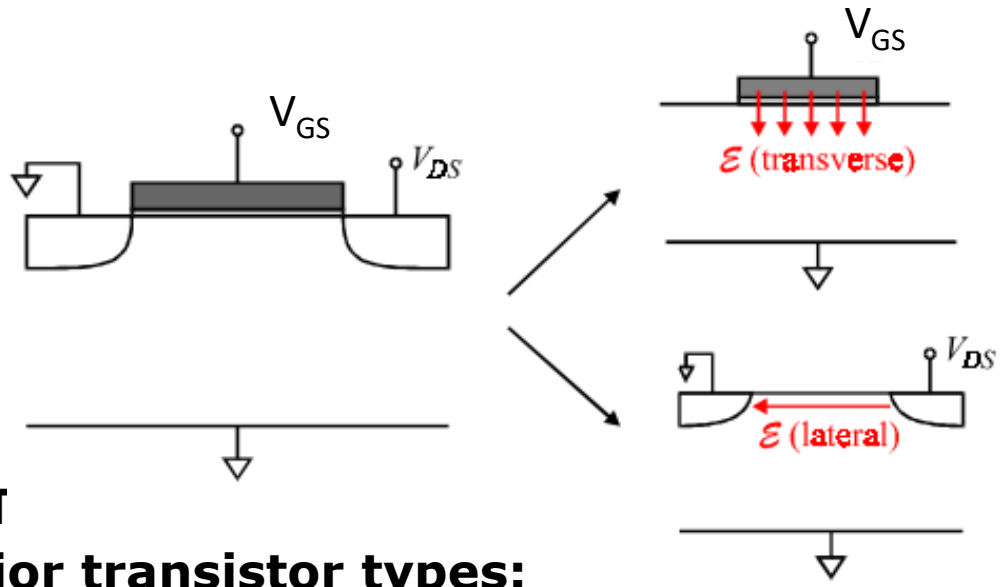
[Vinod Kumar Khanna
"Integrated Nanoelectronics"
Nanoscale CMOS, Post-CMOS
& Allied Nanotechnologies
Springer India 2016]



http://emicroelectronics.free.fr/onlineCourses/VLSI/ch02.html

MOSFET Characteristics (basics)

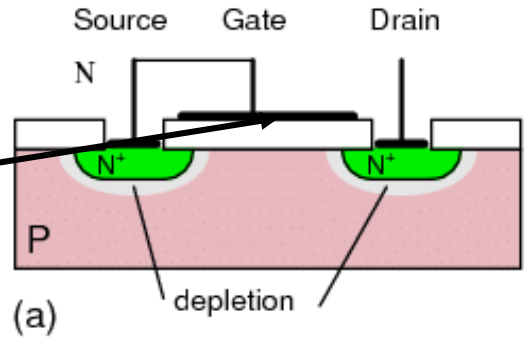
- MOSFET are characterized by
  2 electric field distributions in the structure:
- **The transverse field caused by the potential difference between the gate and the substrate (V_{GS}).** This field supports the substrate depletion region ($V_{GS} < V_{th}$) and inversion layer ($V_{GS} > V_{th}$).
- **The lateral field from source to drain potential (V_{DS}) --> main mechanism for current flow in the MOSFET**

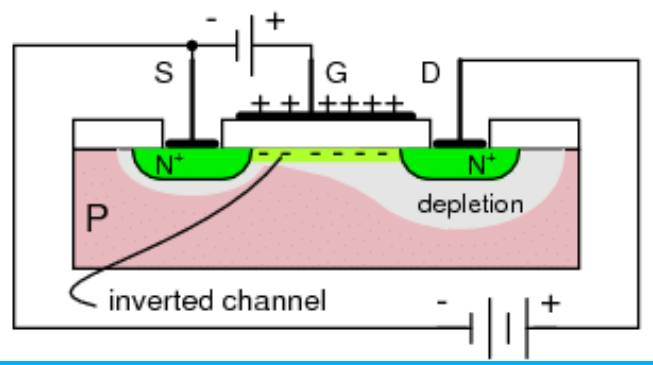


- **Depletion mode and enhancement mode are two major transistor types:**
  - **depletion = transistor in a normally-ON state**
  - **enhancement = transistor in a normally-OFF state**

  } **at zero gate-source voltage**

A depletion region @ zero or low V_{GS}. No current flow through the channel.

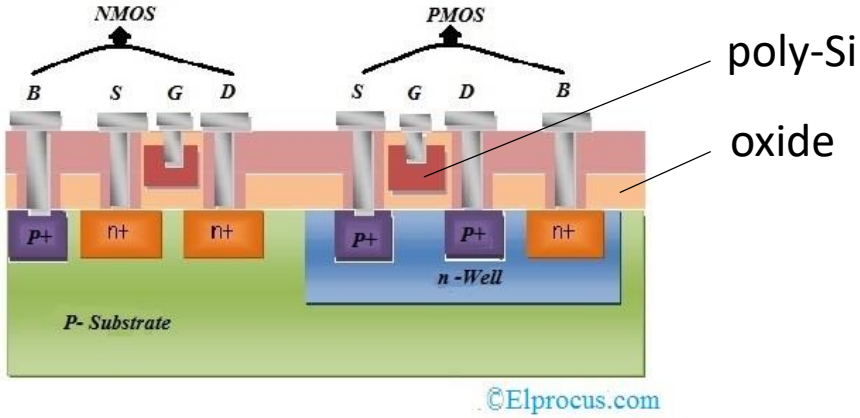


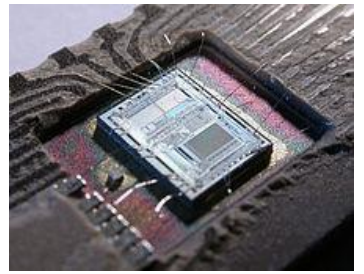


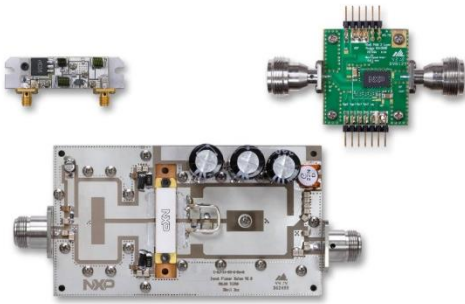
An inversion region with an excess of e- forms below the gate oxide. This region connects the source and drain N-type regions, forming a continuous N-region from source to drain.

Complementary metal–oxide–semiconductor (CMOS)

- **CMOS technology: complementary MOS technology using both N and P channel devices**
- **Advantages of CMOS: high noise immunity & low static power consumption**
- CMOS technology is used to implement **logic gates and other digital circuits in integrated circuit (IC) chips,** such as microprocessors, microcontrollers, memory chips, and other digital logic circuits.
- CMOS technology is also used for **analog circuits** such as image sensors (CMOS sensors), data converters, RF circuits (RF CMOS), and highly integrated transceivers for many types of communication.

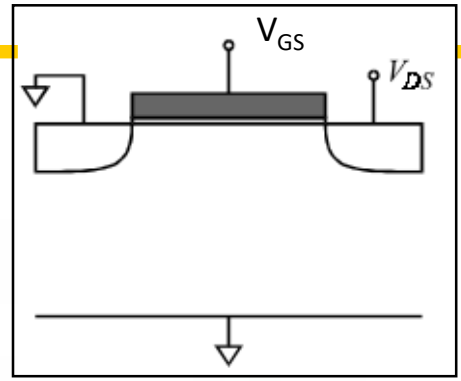






https://en.wikipedia.org/wiki/CMOS#Logic

MOSFET Characteristics (basics)



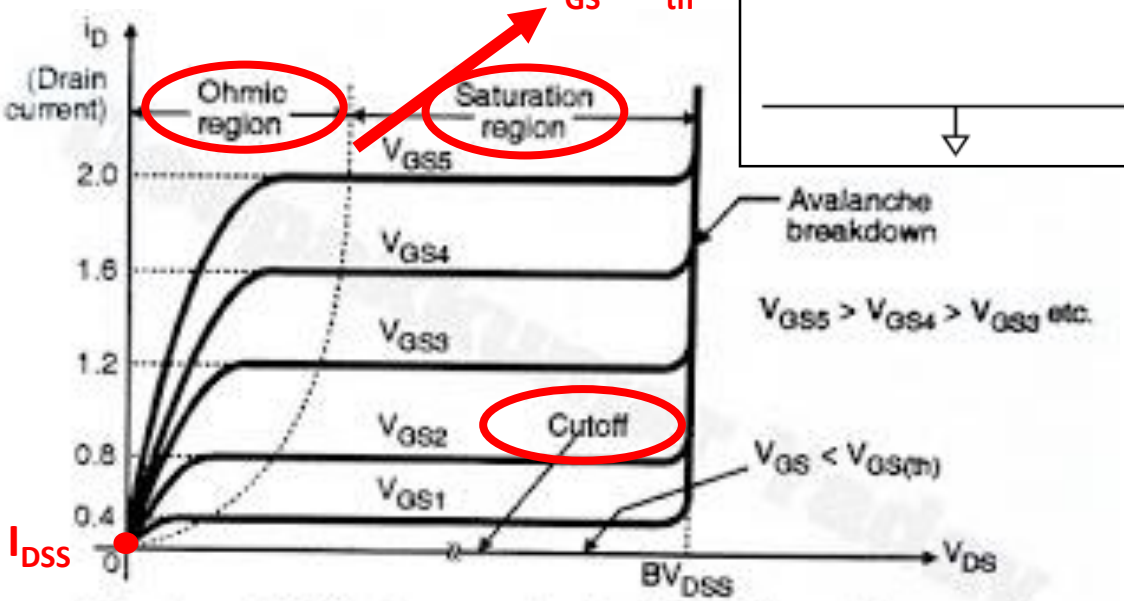
- **The output characteristics represents the drain current i_D vs. drain to source V_{DS} for different values of gate to source voltage V_{GS}**

- **The operation of MOSFET is used in 3 main regions:**

  - **Cut-off region:** the device will be in the OFF condition and NO current flow through it

  - **Linear/Ohmic region:** the current I_D across the drain to source terminal increases linearly with the voltage across the drain to source path

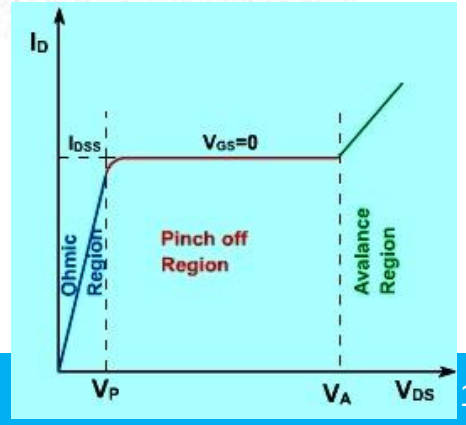
  - **Saturation region:** the device has its drain to source current value I_D constant independent of the value of V_{DS} (the channel is pinched off at the drain side)



Output IV characteristic of n channel enhancement mode

A 4th region occurs as V_{DS} increases beyond V_{DSS} (saturation): the pinch off point moves away from the drain by ΔL and has the effect of changing the effective channel length in the transistor

I_{DSS}: maximum current flowing through when the gate voltage V_{GS} is 0V.

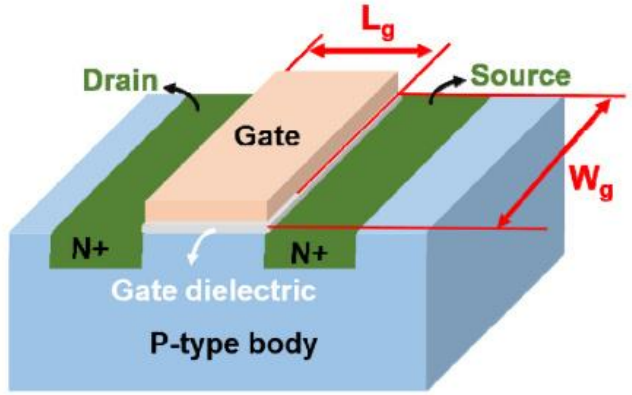


MOSFET Characteristics (basics): amplifier function

- **<u>Linear/Ohmic region:</u> When the MOSFET functions in this region, it works as an amplifier functionality.**
  The ability of MOSFET to amplify the signal is given by the output/input ratio:

  --> transconductance $g_m = (dI_D/dV_{GS})_{VDS} = V_{DS}\mu WC_i/L$

  μ = carrier mobility
  L = gate length
  W = gate width
  C_i = gate insulator capacitance

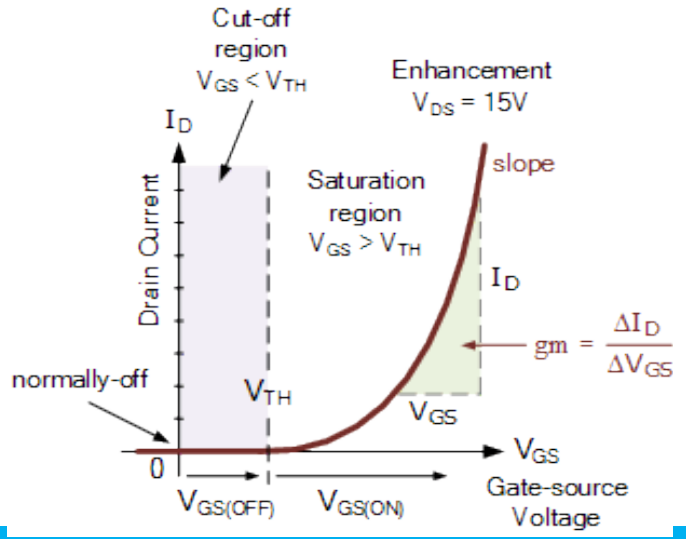


➡ **High transconductance is obtained with high values of:**

- **the low field electron mobility** (i.e. before saturation)
- **thin gate insulator layers**

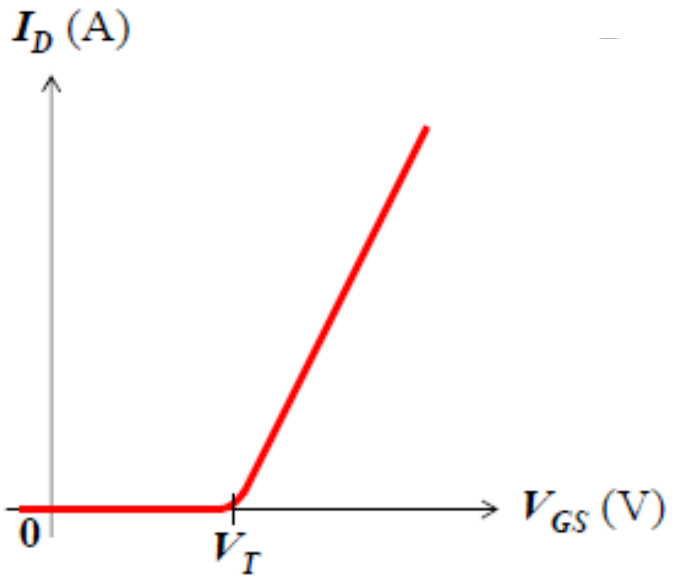
  (i.e. larger gate insulator capacitance $c_i = \varepsilon_i/d_i$ *with*

  ε_i *the permittivity and* d_i *the thickness of the gate dielectric)*
- **large *W/L ratios***

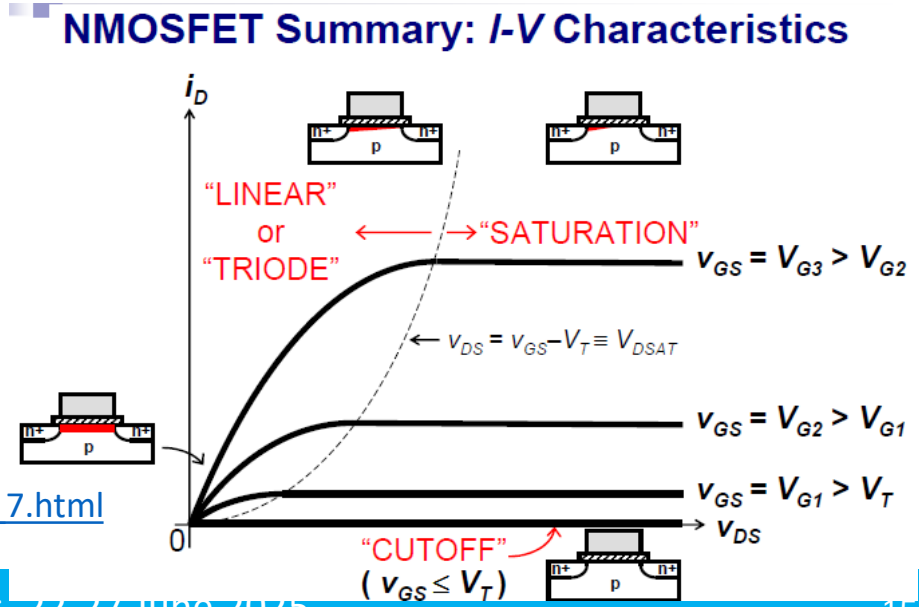


MOSFET Characteristics (basics): switch function

- **MOSFETs widely used as electronic switches** (for controlling loads and in CMOS digital circuits). **They operate in the cut-off or in the saturation region.**
- **<u>Cut-off region:</u>** When V_{GS} is LOW or zero, the channel resistance is very high & the transistor acts like an open circuit --> no current flows through the channel. **The MOSFET is "OFF" operating.**
- **<u>Saturation region:</u>** The ON-state gate voltage V_{GS} that ensures that the MOSFET remains "ON" at the selected drain current I_D can be determined from the V-I transfer curves.
  I_D increases to its maximum value due to a reduction in the channel resistance.
  & becomes constant independently of V_{DS} (it depends only on V_{GS}).
  Therefore, the transistor is "ON" operating and behaves like a closed switch.



https://www.electronics-tutorials.ws/transistor/tran_7.html



From Integrated Circuit…

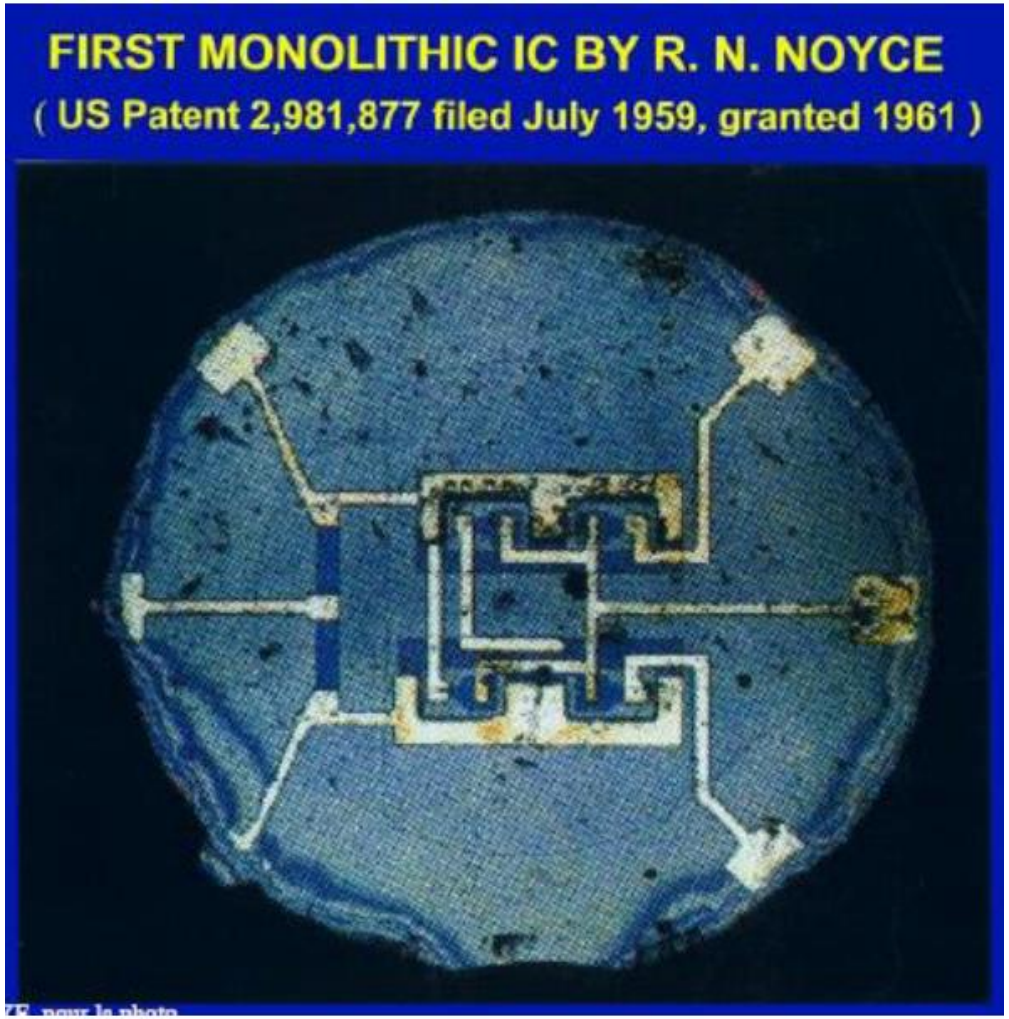
- **IC = a set of electronic circuits on one small flat piece (or "chip") of semiconductor (Si)**

- **The first monolithic IC was produced on May 26th 1960**

Real size
1/1 scale size

¼ of 2-inch

→ **Fabrication of all the components (transistors & resistances) on a same wafer by using oxide and Al contacts**



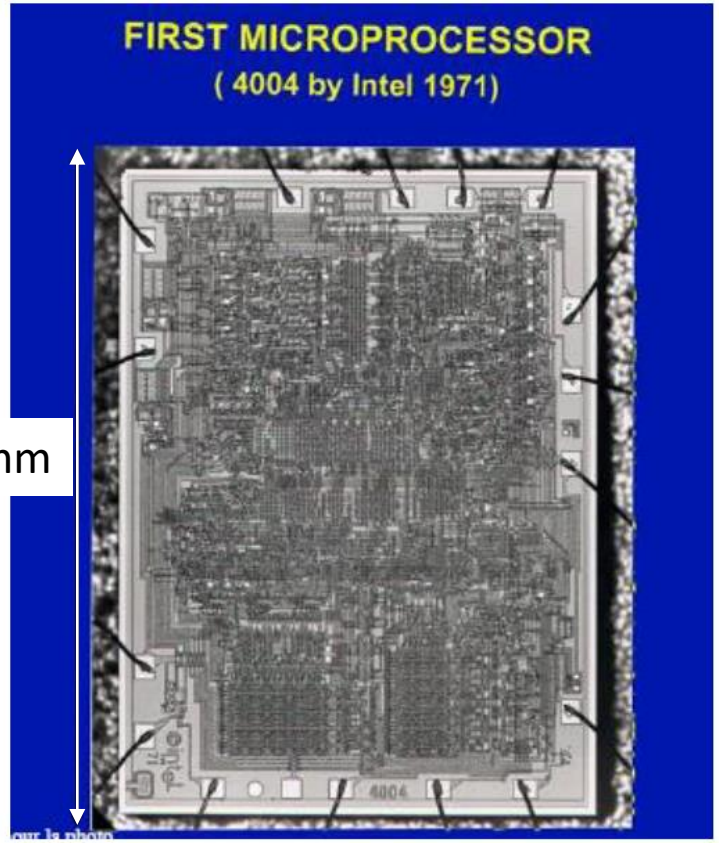
¼ of 2-inch

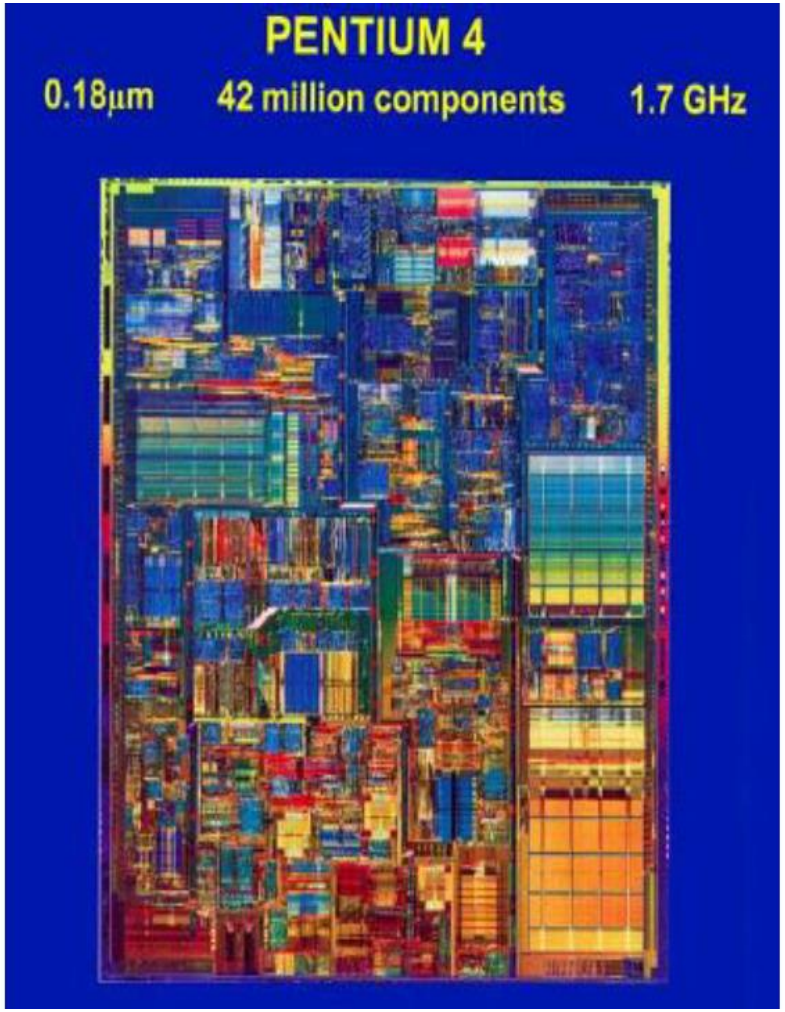
Robert Norton Noyce, co-founder of Fairchild Semiconductor in 1957 and Intel Corporation in 1968

… to Microprocessor

- **First Microprocessor in 1971 (few thousands of MOS transistors)**
- **Pentium 4 in 2000 (42 millions of components)**

Real size
1/1 scale size



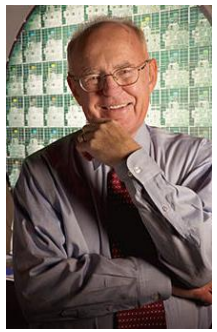


Moore's Law & Scaling Rules

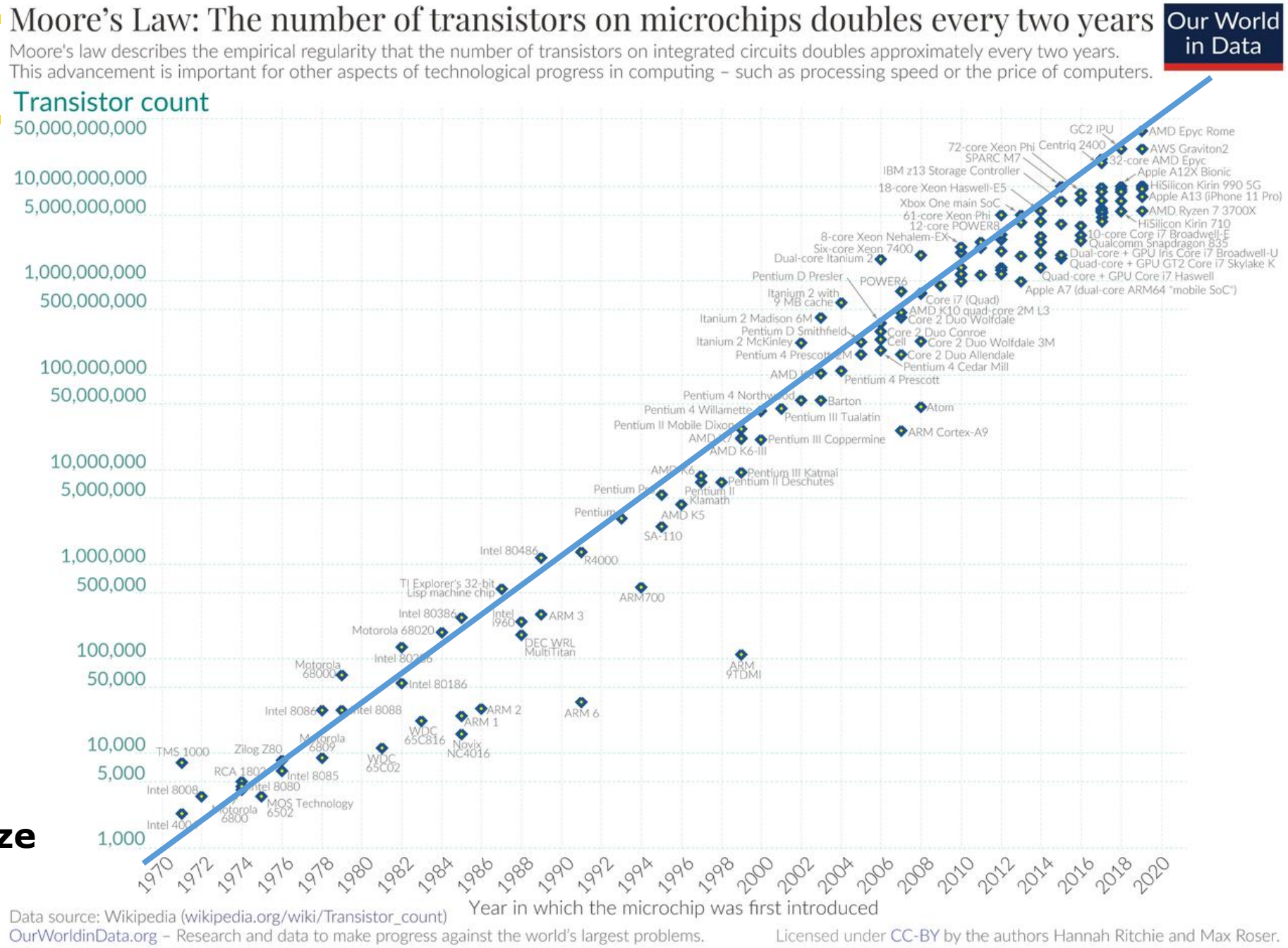
Moore’s Law

- **Moore’s Law:**

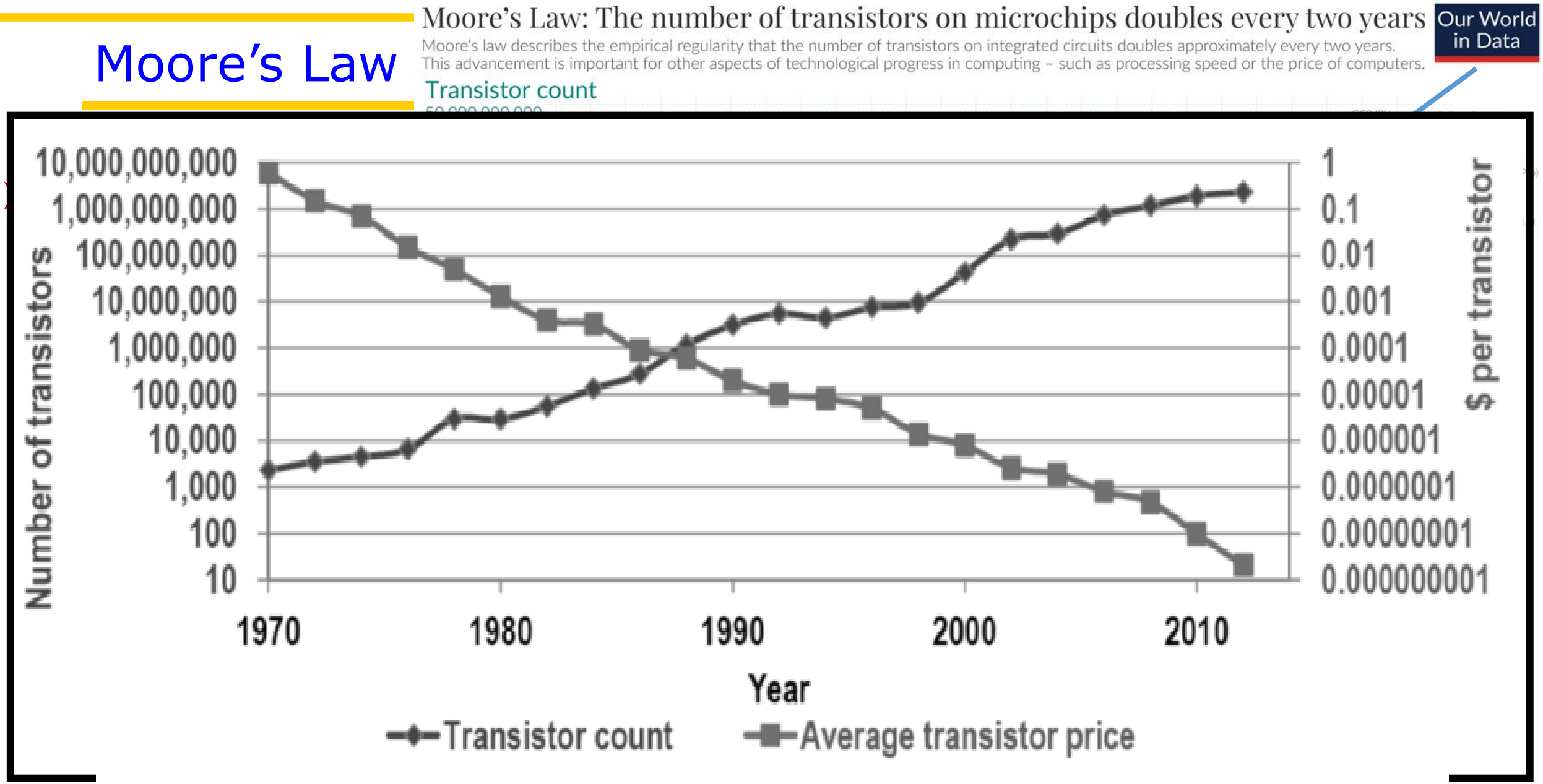
“Doubling in the number of components per integrated circuit (every 1.5 to 2-years)”
Gordon Moore (1965)



- **Reduction of the size of the MOSFET**



Moore's Law



➡ **The fabrication cost is divided by 10 every ~5 years**

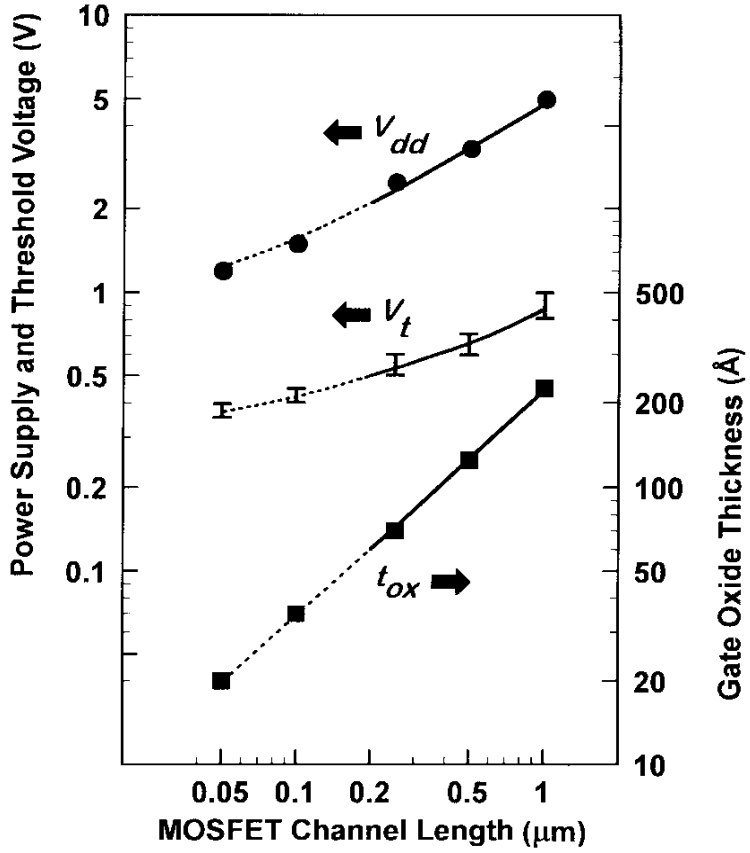
Transistor dimensions & performances

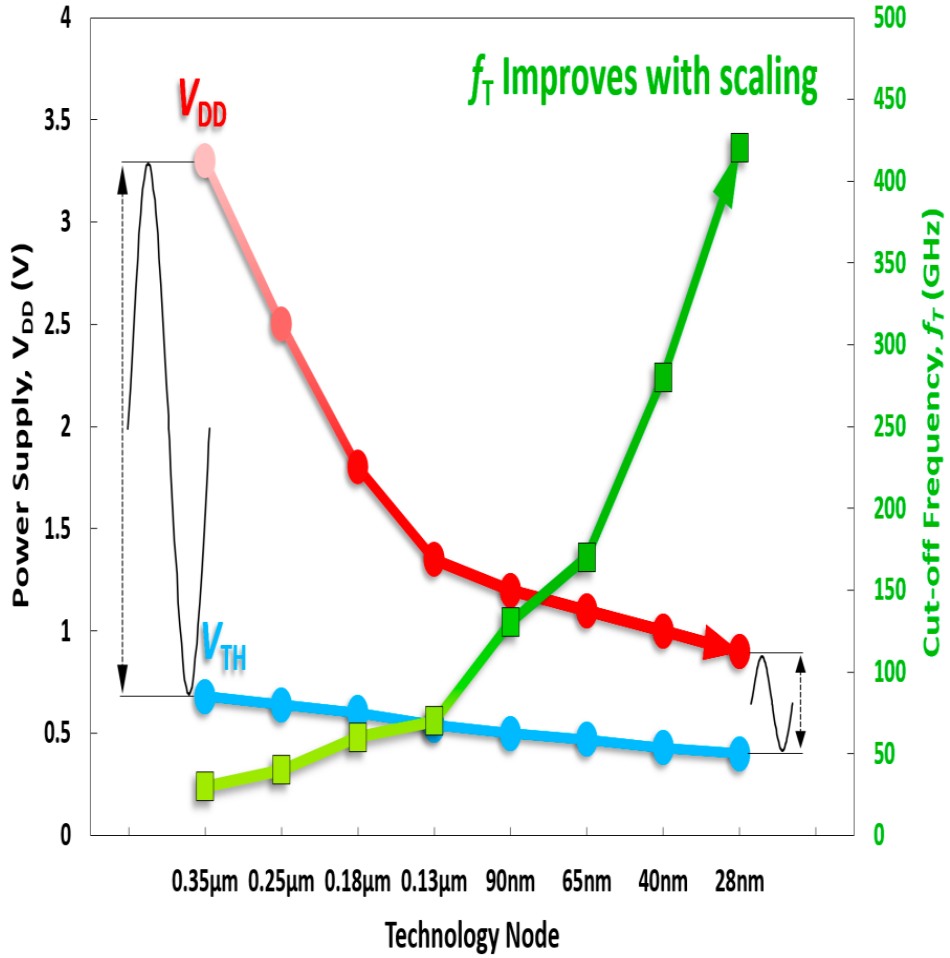
- **Following the scaling rules has a strong impact on the MOSFET performances**

V_{dd} : operating voltage

V_{th} (V_T): threshold voltage

t_{ox} : oxide thickness





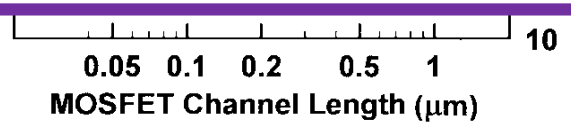
➡ **Increase of the maximum operating frequency**

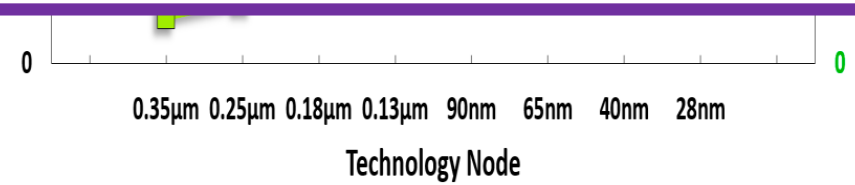
Transistor dimensions & performances

- **Following the scaling rules has a strong impact on the MOSFET performances**

Shrinking of the silicon transistors present multiple benefits:

- **a lower power consumption,**
- **increased performance** (i.e. faster transistors operating at higher frequencies)
- **increasing functionality** (primary by increasing the transistor density)
- **a reduction in the fabrication cost per transistor…**





Transistor dimensions & performances

- **Following the scaling rules has a strong impact**

Proper scaling of MOSFET requires:

- a size reduction of the gate length and width **but NOT only**

--> it requires a reduction of all other dimensions

- **including the gate/source and gate/drain alignment,**
- **the oxide thickness and the depletion layer widths,**
- **Scaling of the substrate doping density…**

Technology Node

Scaling rules

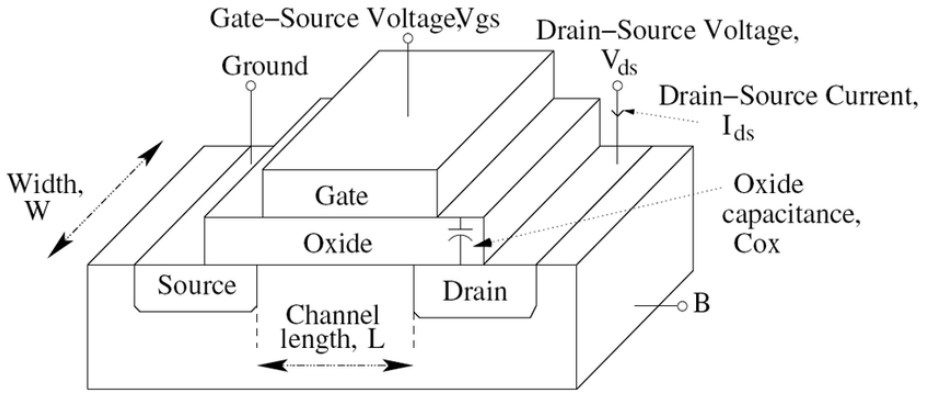
- **A CMOS technology generation has:**
  - **a minimum channel length and width (L & W),**
  - **an oxide thickness t_{ox},**
  - **a substrate doping N_A,**
  - **a power supply voltage V_{DD},**
  - **a threshold voltage V_{th}, etc.**

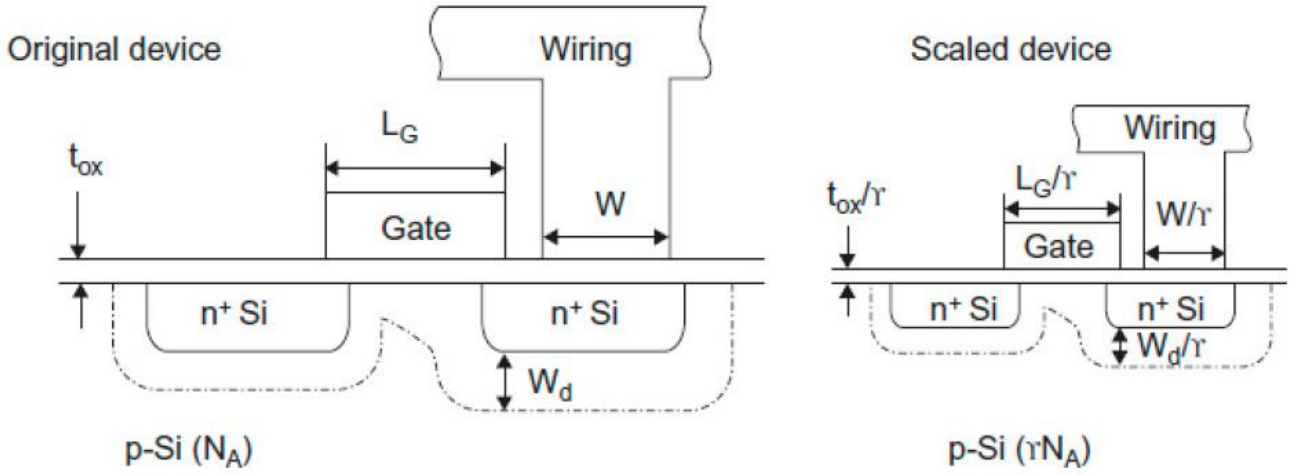
- **Downscaling: gate length and width, oxide thickness, junction depth, and substrate doping.**

Supply and threshold voltages are also scaled by a factor of γ (or S).

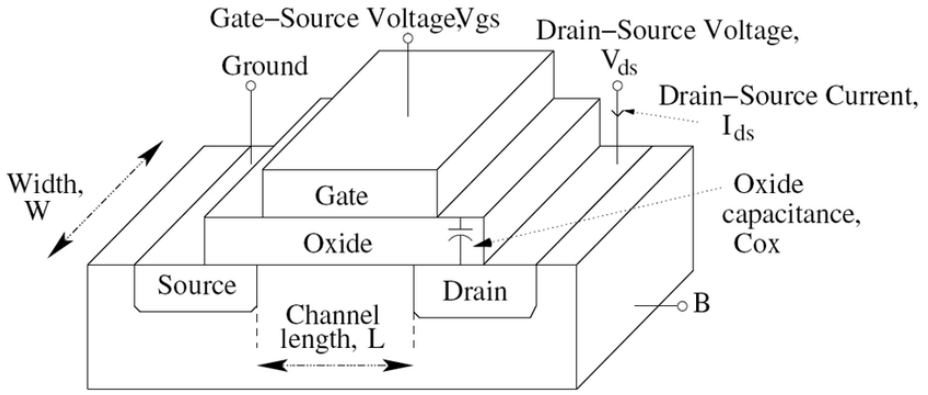
The electric field is constant.
(rules developed by Robert Dennard in 1974).

The transistor density is increased by a factor of γ^2.





Scaling rules

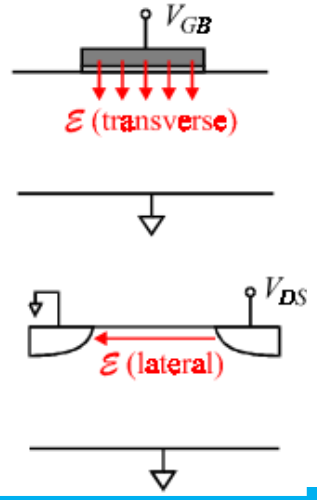


- **Two types of scaling (S = 1/0.7) can be used:**

1) constant voltage scaling

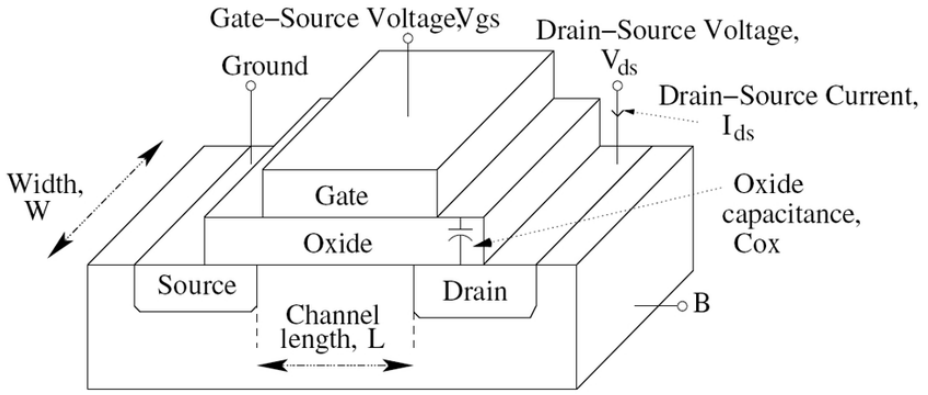
➡ **Avoid the reduction in V_{DD} and V_{th} = preferred scaling method since it provides voltage compatibility with older circuit technologies.**

However, the disadvantage of constant voltage scaling is that the electric field increases as the minimum feature length is reduced. This leads to velocity saturation, mobility degradation, increased leakage currents and lower breakdown voltages.



After Constant Voltage Scaling
$L' = L/s$
$W' = W/s$
$t'_{ox} = t_{ox}/s$
$x'_i = x_i/s$
$V'_{DD} = V_{DD}$
$V'_{Th} = V_{Th}$
$N'_a = N_a * s^2$ or $N'_d = N_d * s^2$
$C'_{ox} = C_{ox} * s$
$I'_{DS} = I_{DS} * s$
$P'_D = P_D * s$

Scaling rules



- **Two types of scaling (S = 1/0.7) can be used:**

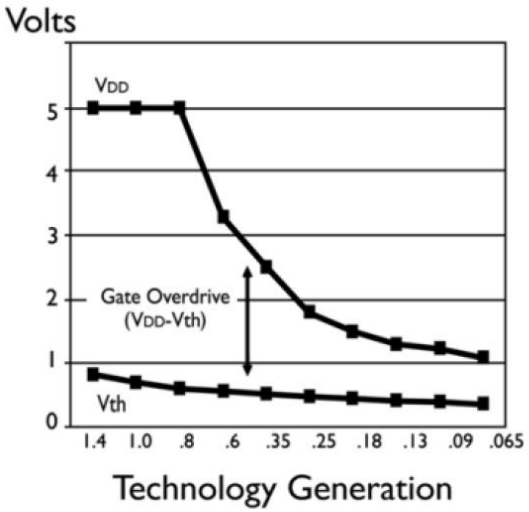
2) constant field scaling (Dennard's scaling – dictates the CMOS scaling technology)

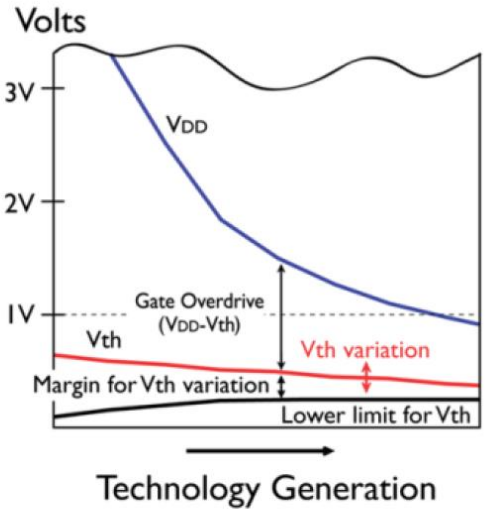
➡ **requires a reduction in V_{DD} as one decreases the minimum feature size.**

Difficulty of lowering V_{th}

Limit of MOSFET operation with a minimum overdrive voltage ($V_{DD} - V_{th}$)

After Constant Field Scaling
$L' = L/s$
$W' = W/s$
$t'_{ox} = t_{ox}/s$
$x'_i = x_i/s$
$V'_{DD} = V_{DD}/s$
$V'_{Th} = V_{Th}/s$
$N'_a = N_a * s$ or $N'_d = N_d * s$
$C'_{ox} = C_{ox} * s$
$I'_{DS} = I_{DS}/s$
$P'_D = P_D/s^2$





[Trans. Electr. Electron. Mater. 11(3) 93 (2010): Y.-B. Kim]

Fig. 1. Trend of supply voltage and threshold voltage scaling.

Trade-off between performance & high-density → leakage power dissipation (increases by S^{-2})

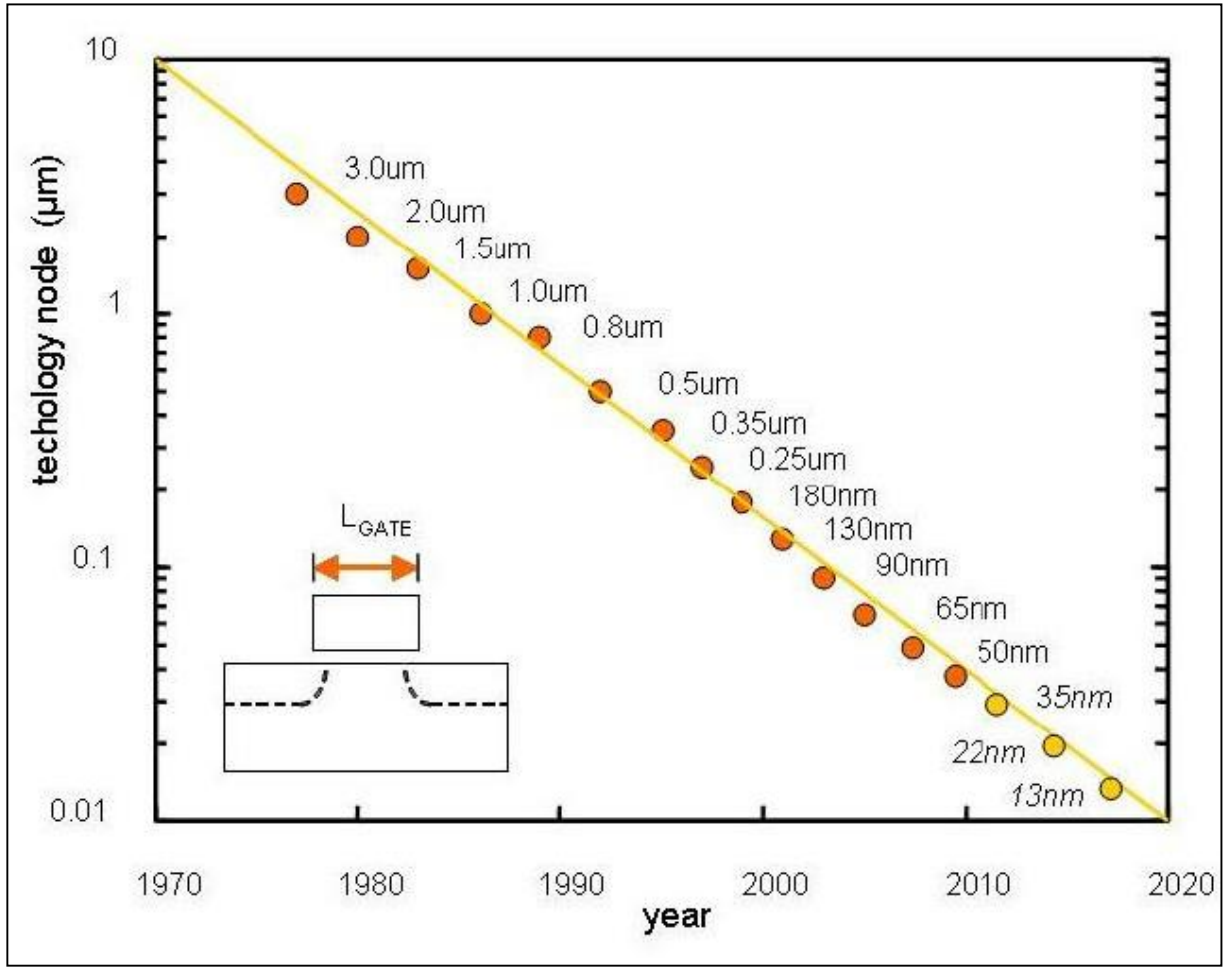
Limit in the Reduction of the transistor size

- **Evolution of the MOSFET transistor channel since 1970**

  Technology node (L_{gate})

- **As of 1980, the size reduction has been exponential**

- **Scaling to keep up with the demand for faster, smaller, cheaper products without any significant changes, relying on improved lithography processes** (used to transfer the electronics network patterns to every layer of IC)



Limit in the Reduction of the transistor size

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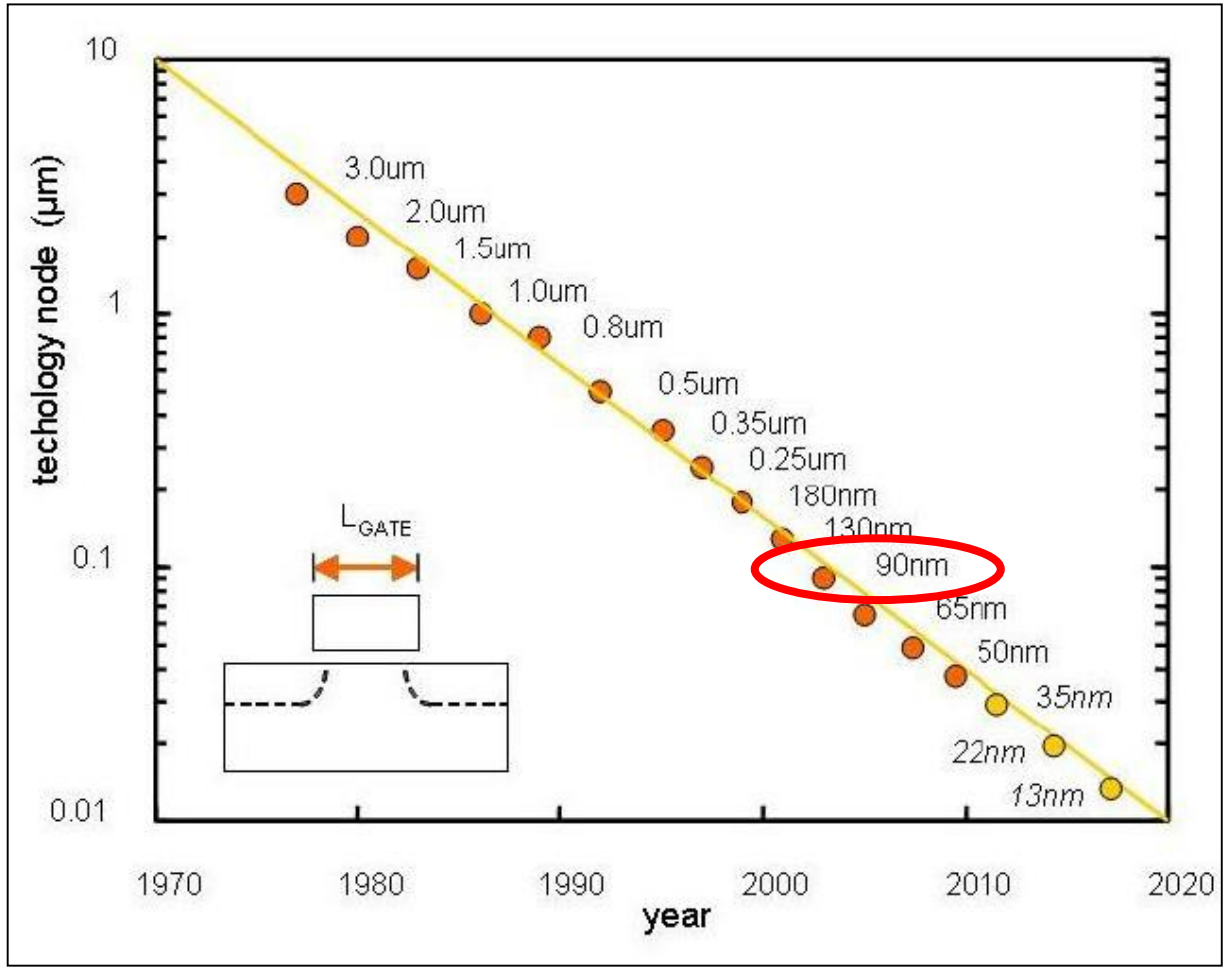
- **As the technology node reached 90 nm (in 2005), challenges started to appear !** ⟶ **nano-electronic era**



Limit in the Reduction of the transistor size

- **Evolution of the MOSFET transistor channel since 1970**

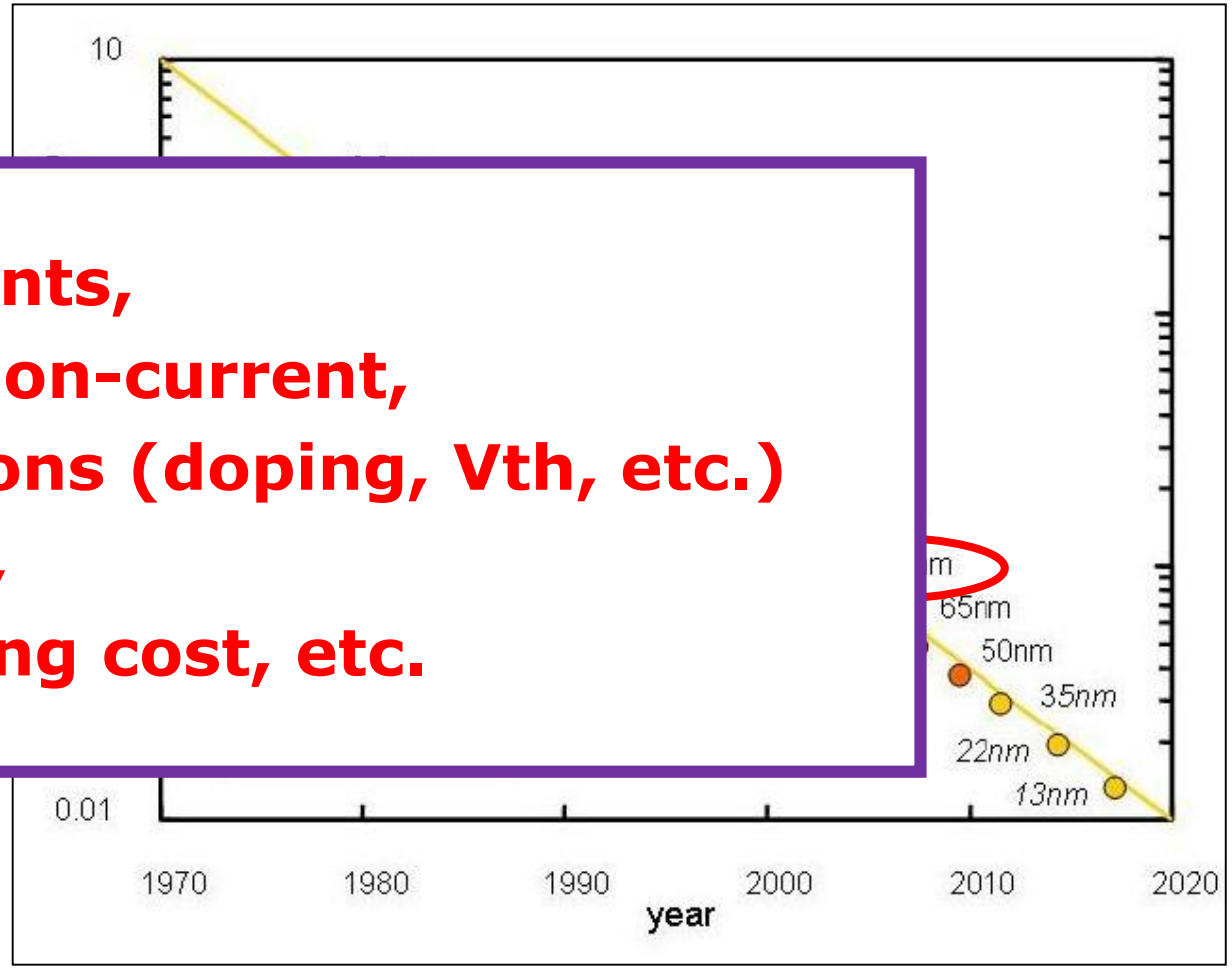
- **Techn**

- **As of 19 has bee**

- **Scaling for faste without relying** (used to patterns

- **As the technology node reached 90 nm (in 2005), challenges started to appear !** → **nano-electronic era**

Increased leakage currents,
Difficulty on increase of on-current,
Large parameter variations (doping, Vth, etc.)
Low reliability and yield,
Increase in manufacturing cost, etc.

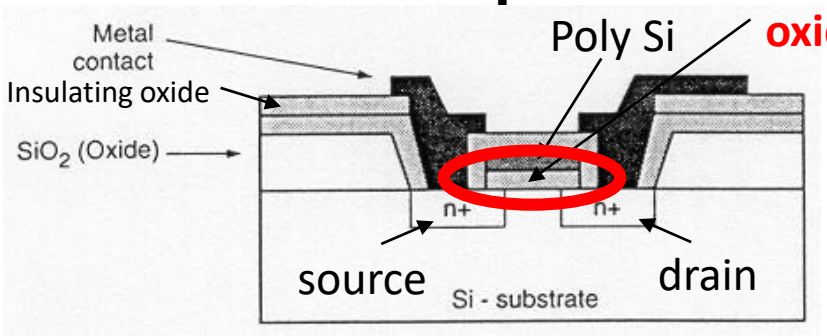


The Beginning of Heterogeneous Integration

Gate technology vs. Leakage current

- **From the original CMOS technology, the introduction of new materials is required**

The SiO_2 layer used as the gate oxide became extremely thin (~1.2 nm) ⟹ difficulty to precisely control the thickness & **the gate leakage current** (due to direct tunneling of electrons through the SiO_2) **becomes too high** (> 1 A/cm² at 1 V)



The gate oxide layer was the first element to reach the physical limit

- **A FET is operated through the gate capacitance, which is expressed as**

$$C = (\varepsilon_0 \times K \times A) / t$$

with ε_0 = permittivity of free space, K = relative dielectric const., A = area & t = oxide thickness

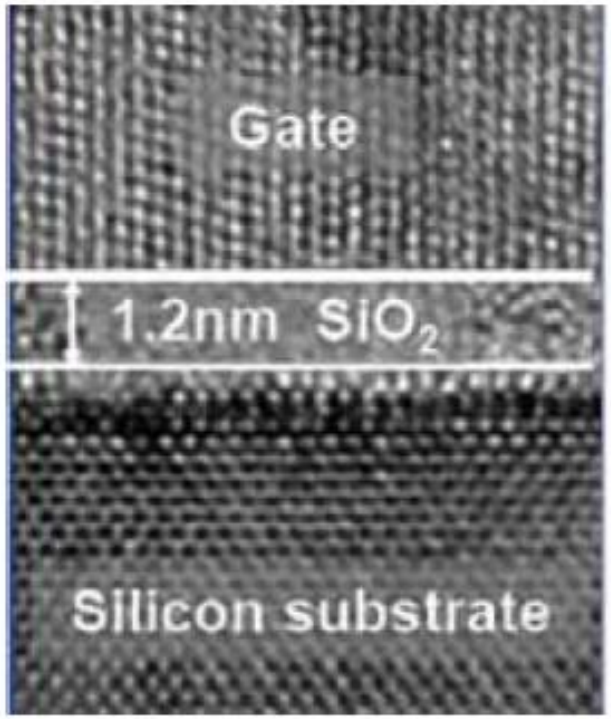
⟹ **Solution: to replace SiO_2 with a thicker layer of new material of higher K to keep the same capacitance, but decrease the tunneling current with new gate 'high K oxides':**

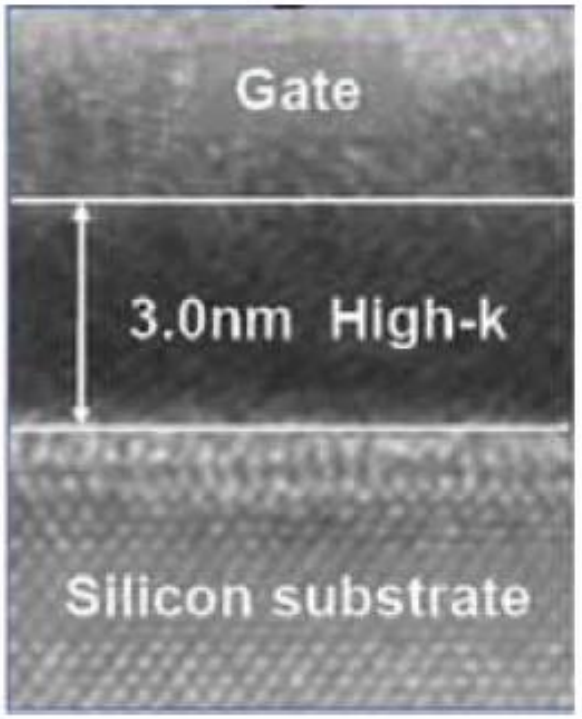
Equivalent oxide thickness: $\mathbf{t_{ox} = EOT = (3.9/K) \times t_{HiK}}$ (with $K_{SiO2} = 3.9$)

High-K gate dielectric Materials

Table 1. Static dielectric constant (K), experimental band gap and (consensus) conduction band offset on Si of the candidate gate dielectrics.

	K	Gap (eV)	CB offset (eV)
Si		1.1	
SiO_2	3.9	9	3.2
Si_3N_4	7	5.3	2.4
Al_2O_3 sapphire	9	8.8	2.8
Al_2O_3 ALD	8	6.4	1.6
Ta_2O_5	22	4.4	0.35
TiO_2	80	3.5	0
$SrTiO_3$	2000	3.2	0
ZrO_2	25	5.8	1.5
HfO_2	25	5.8	1.4
$HfSiO_4$	11	6.5	1.8
La_2O_3	30	6	2.3
Y_2O_3	15	6	2.3
a-$LaAlO_3$	30	5.6	1.8
$LaLuO_3$	32	5.2	2.1





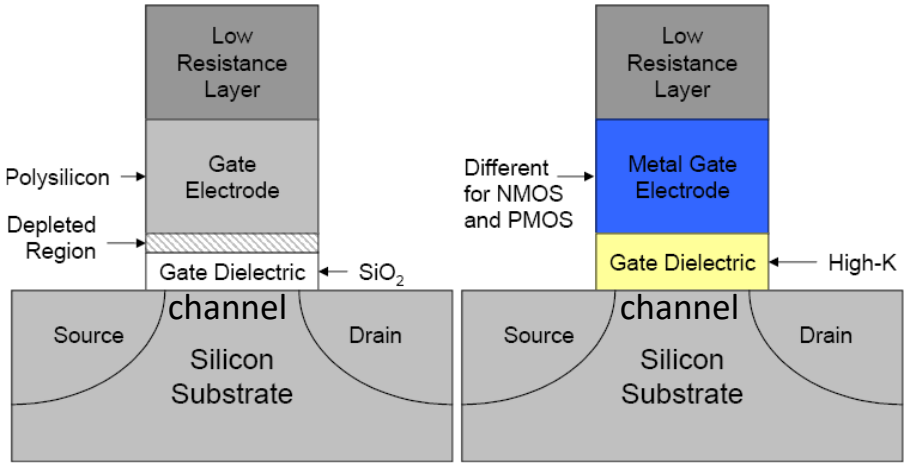
→ **t_{ox} = EOT = (3.9/K) x t_{HiK}**
HfO_2 is the most suitable choice

[J. Robertson et al.,
Materials Science and Engineering: R: Reports 88 pp. 1-41 (2015)]

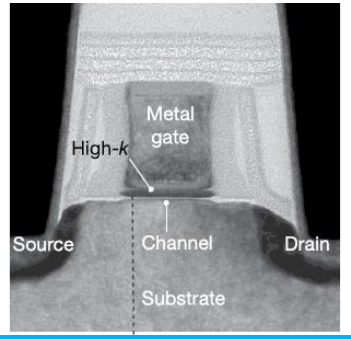
A new technology of transistors: HKMG

➢ **After changing the gate dielectric material, another required change was the gate electrode as it was leading to degraded performances (switching speed, threshold voltage …)**

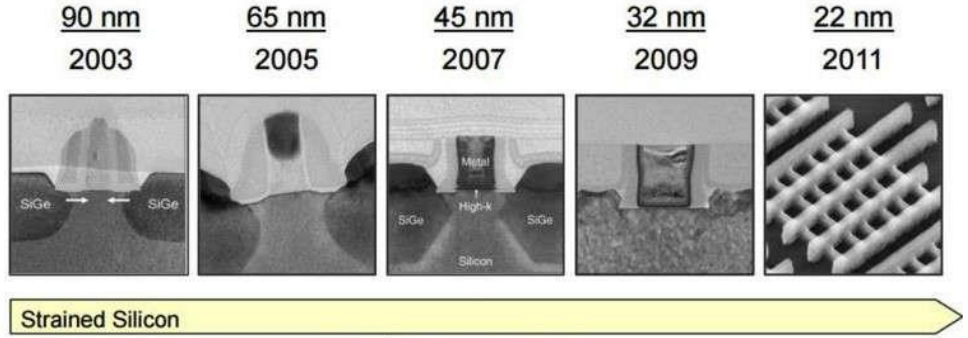
Development of metal gates
(reduction of gate leakage currents, lower resistance, threshold voltage control)



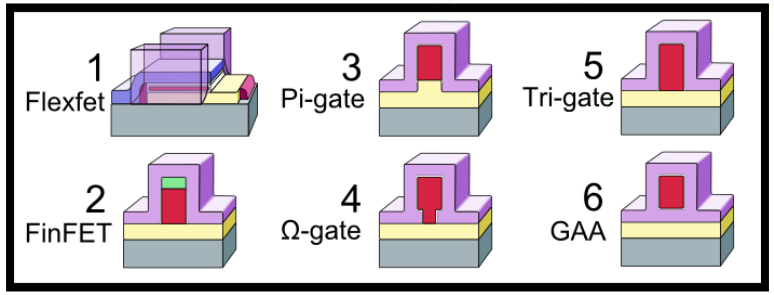
[M. Wang, J. Phys.: Conf. Ser. 2798 012039 (2024)]



[W. Cao et al., Nature 620, 501 (2023)]



Source: Intel



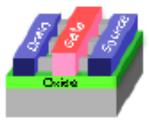
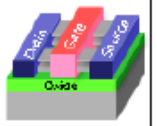
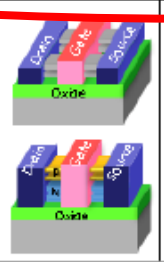
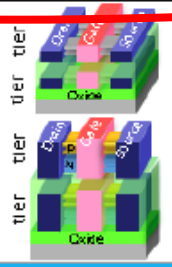
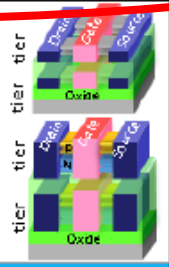
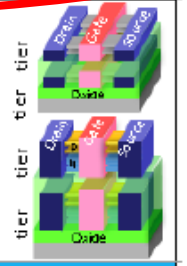
New design: Multi-gate technology

https://huniv.hongik.ac.kr/~hmed/nanofet.html

By Multigate_models_2.PNG: Shigeru23derivative work: Cepheiden (talk) - Multigate_models_2.PNG, CC BY-SA 3.0, https://commons.wikimedia.org/w/index.php?curid=17815945

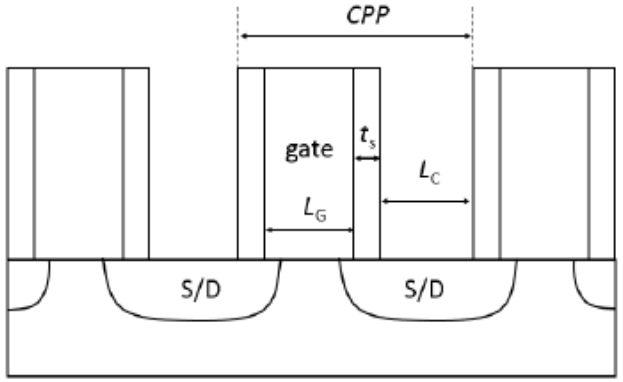
IRDS nodes from 2023 to 2037

- **IRDS** (Int. Roadmap for Devices and Systems) **2023**

YEAR OF PRODUCTION	2022	2025	2028	2031	2034	2037
	G48M24	G45M20	G42M16	G40M16/T2	G38M16/T4	G38M16/T6
Logic industry "Node Range" Labeling	"3nm"	"2nm"	"1.5nm"	"1.0nm eq"	"0.7nm eq"	"0.5nm eq"
Fine-pitch 3D integration scheme	Stacking	Stacking	Stacking	3DVLSI	3DVLSI	3DVLSI
Logic device structure options	finFET LGAA	LGAA	LGAA CFET-SRAM	LGAA-3D CFET-SRAM	LGAA-3D CFET-SRAM	LGAA-3D CFET-SRAM
Platform device for logic	finFET	LGAA	LGAA CFET-SRAM	LGAA-3D CFET-SRAM-3D	LGAA-3D CFET-SRAM-3D	LGAA-3D CFET-SRAM-3D
						
LOGIC DEVICE GROUND RULES						
Mx pitch (nm)	32	24	20	16	16	16
M1 pitch (nm)	32	23	21	20	19	19
M0 pitch (nm)	24	20	16	16	16	16
Gate pitch (nm)	48	45	42	40	38	38
Lg: Gate Length – HP (nm)	16	14	12	12	12	12
Lg: Gate Length – HD (nm)	18	14	12	12	12	12
Channel overlap ratio – two-sided	0.20	0.20	0.20	0.20	0.20	0.20
Spacer width (nm)	6	6	5	5	4	4
Spacer k value	3.5	3.3	3.0	3.0	2.7	2.7
Contact CD (nm) - finFET, LGAA	20	19	20	18	18	18
Device architecture key ground rules						
Device lateral pitch (nm)	24	26	24	24	23	23
Device height (nm)	48	52	48	64	60	56
FinFET Fin width (nm)	5.0					
Footprint drive efficiency - finFET	4.21					
Lateral GAA vertical pitch (nm)		18.0	16.0	16.0	15.0	14.0
Lateral GAA (nanosheet) thickness (nm)		6.0	6.0	6.0	5.0	4.0
Number of vertically stacked nanosheets on one device		3	3	4	4	4
LGAA width (nm) – HP		30	30	20	15	15
LGAA width (nm) – HD		15	10	10	6	6
LGAA width (nm) – SRAM		7	6	6	6	6
Footprint drive efficiency – lateral GAA – HP		4.41	4.50	5.47	5.00	4.75
Device effective width (nm) – HP	101.0	216.0	216.0	208.0	160.0	152.0
Device effective width (nm) – HD	101.0	126.0	96.0	128.0	88.0	80.0
PN separation width (nm)	45	40	20	15	15	10

Modification/improvement of the device design

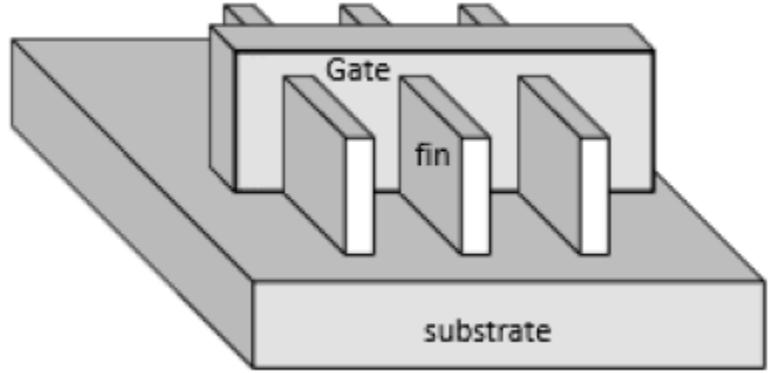
Adoption of FinFET technology in volume production at 22 nm node (2012)



[K. Cheng et al., ECS Transactions 80, 17 (2017)]

FinFET Technology

- A fin field-effect transistor is a multigate device MOSFET built on a substrate where the gate is placed on 2, 3, or 4 sides of the channel or wrapped around the channel, forming **a double or even multi gate FET**
--> technology started to be implemented in 2011



- **Excessive reduction of the gate length (L_G) in conventional MOSFET leads to an increase of the leakage current**
--> excessive stand-by power consumption.

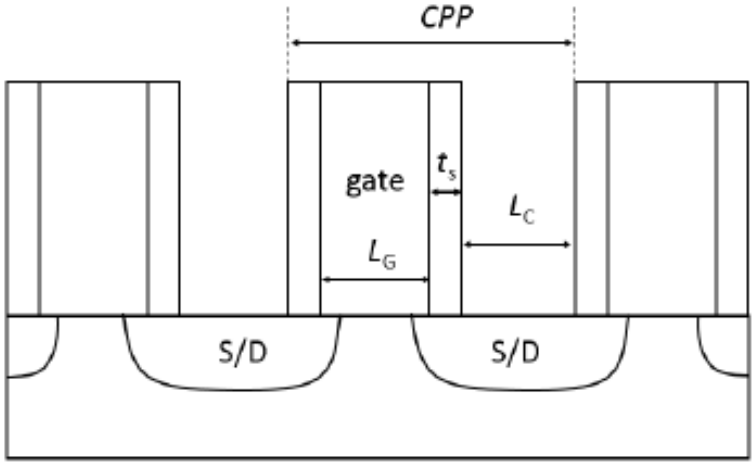
- **FinFET has improved electrostatics enabling the further scaling of L_G and of contact gate pitch (CPP).**

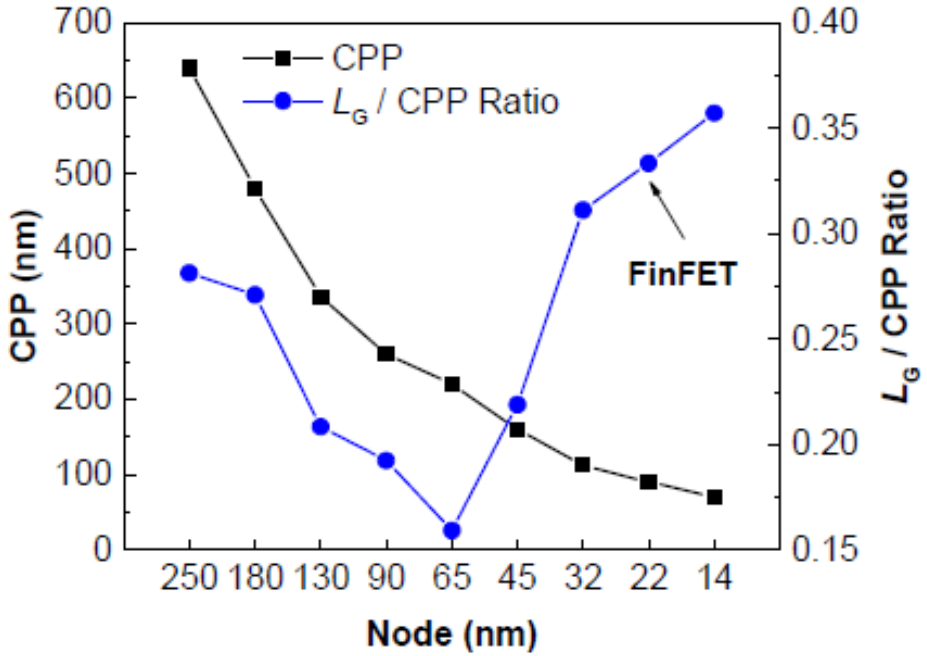
Reduction of V_{th}

active power consumption
(reduction of V_{DD})

performances
(@cst $P_{consumption}$)

[K. Cheng et al., ECS Transactions 80, 17 (2017)]

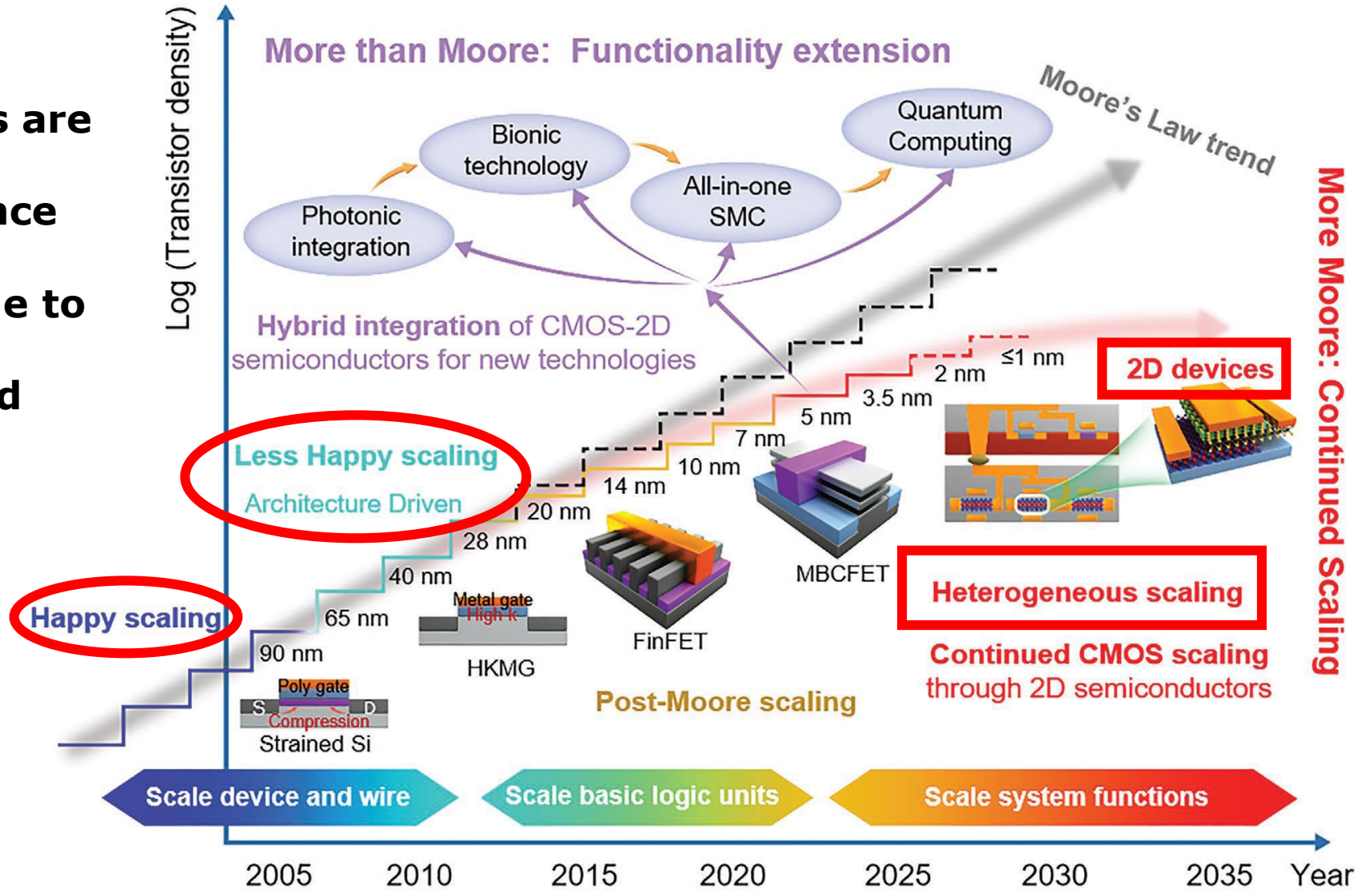




The Challenges of Scaling

"As the transistor dimensions are reaching physical limits, the fabrication of high-performance devices and ICs using scaling rules becomes impossible, due to unsustainable challenges in scaling, energy efficiency, and memory limitations".

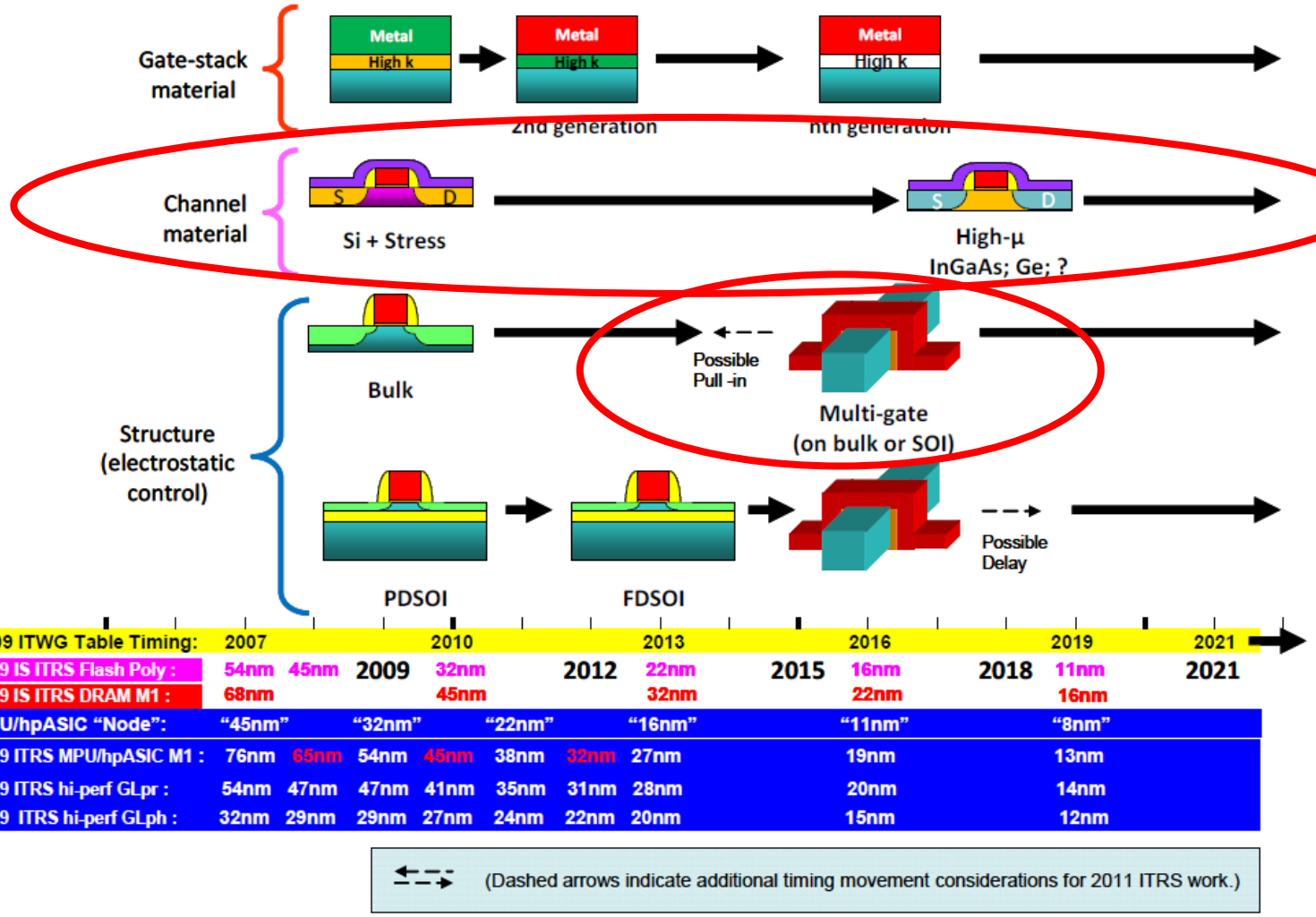
[S. Wang et al., Adv. Materials **34**, 2106886 (2022)]



(Advanced) Heterogeneous Integration

Improvement of the Performances

- **ITRS** (Int. Tech. Roadmap for Semicond.) **2010**



Heterogeneous integration

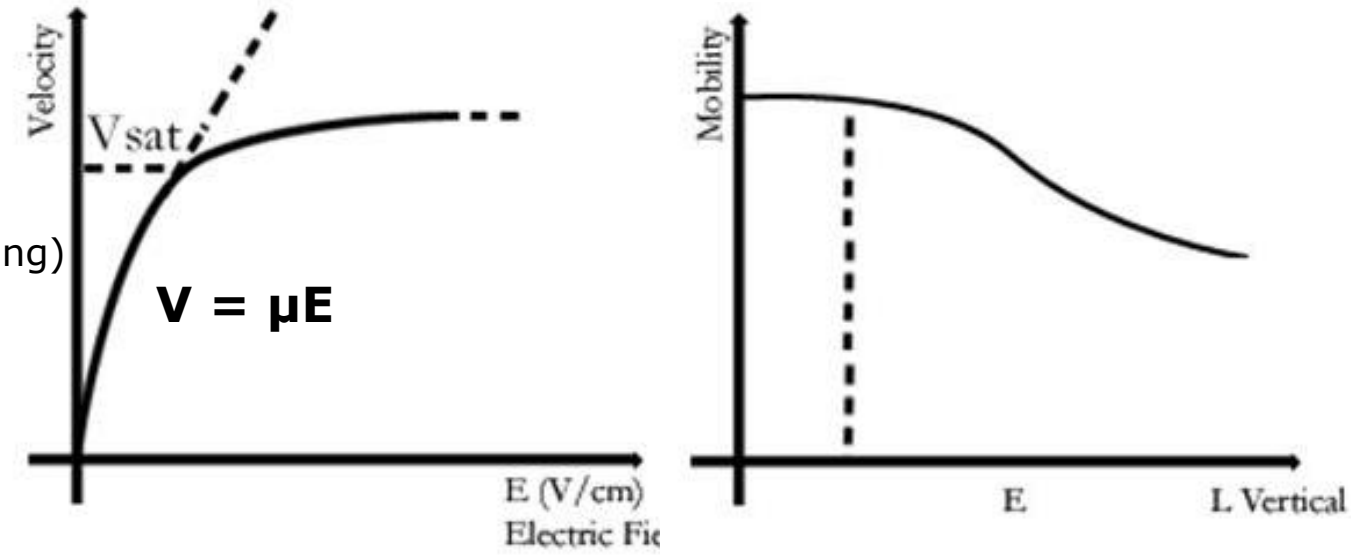
- **High mobility materials (SiGe, III-V)**

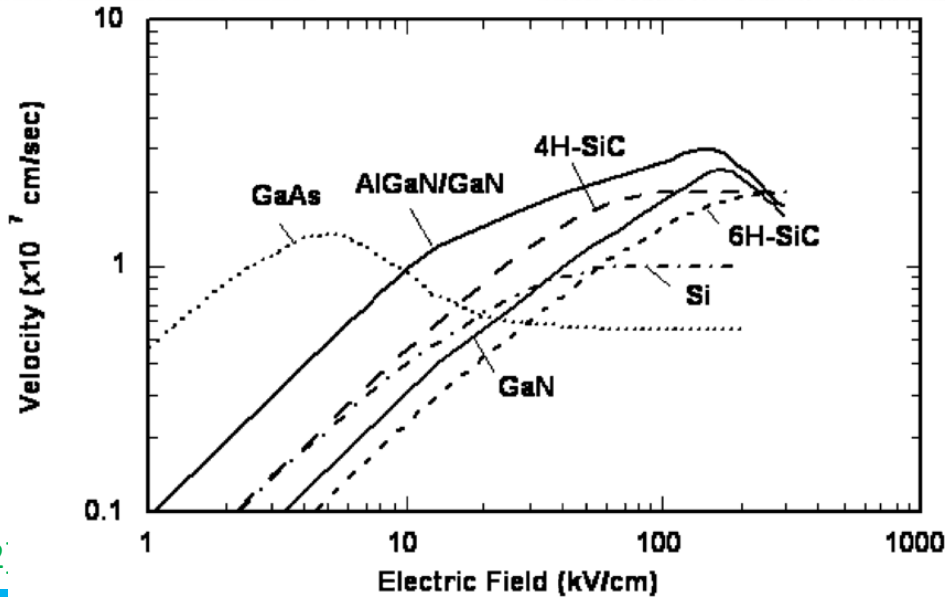
Introduction on a Si platform and a multi-gate based technology

--> Compatibility with the FinFET-based technology

Velocity Saturation & Mobility Degradation

- The electron drift velocity in the channel is **proportional to the electric field @ low electric field values.**
- **It starts to saturate at high E** (phonon scattering) ➡ **velocity saturation (Vsat).**
- For short channel devices, the lateral electric field increases. **At high E, the velocity saturation affects I-V characteristics of the MOSFET.**
- For the same V_{GS} (gate voltage), the saturation mode is achieved at smaller values of V_{DS} and leads to saturation current limitations.
- Due to **higher vertical electric fields**, the carriers of the channel scatter off of the oxide interface. ➡ **This results in the degradation of carrier mobility and the reduction in drain current.**





[R. Trew, « High-Frequency Solid-State Electronic Devices », IEEE Trans. on Elec. Devices(2005), 10.1109/TED.2005.845862]

Velocity Saturation & Mobility Degradation

- The electron drift velocity in the channel is **proportional to the electric field @ low electric field values.**
- **It starts to**
  → **velo**
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  characteri
- For the sam
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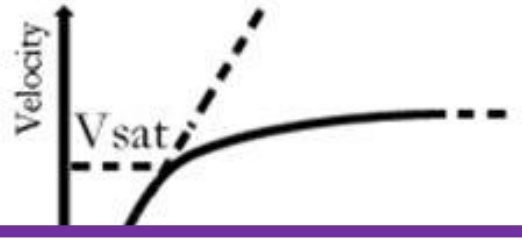
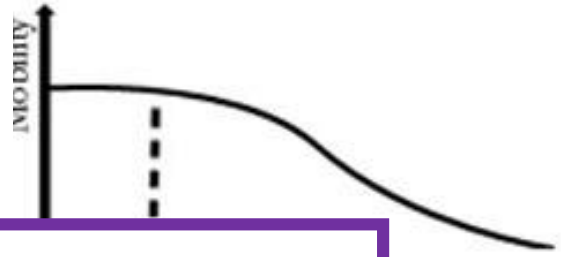
- Due to **high**, the carriers of the channel scatter off of the oxide interface.
  → **This results in the degradation of carrier mobility and the reduction in drain current.**





Both the saturation field & saturation velocity of a semiconductor material are typically strong function of:

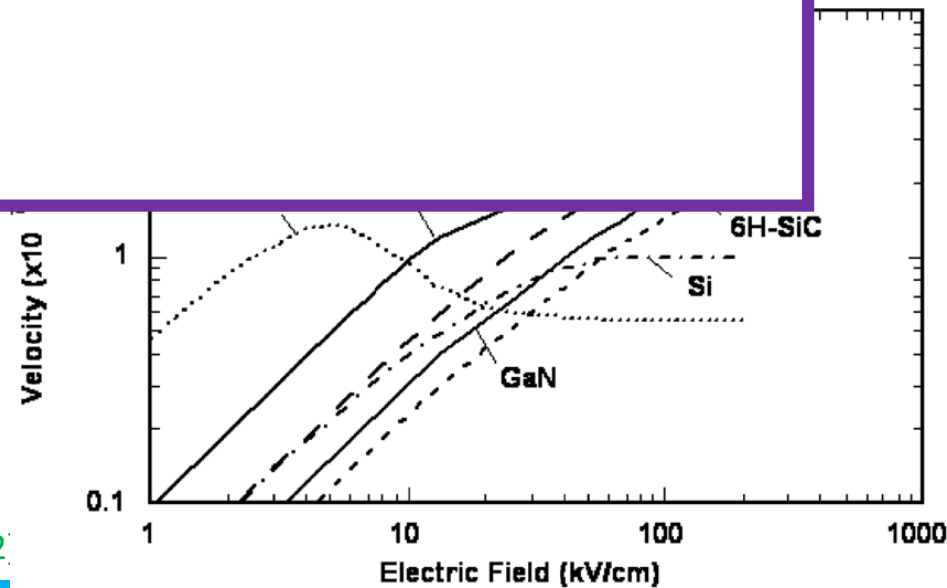
- impurities,

- crystal defects,

- temperature.

L Vertical

RADATION



[R. Trew, « High-Frequency Solid-State Electronic Devices », IEEE Trans. on Elec. Devices(2005), 10.1109/TED.2005.845862]

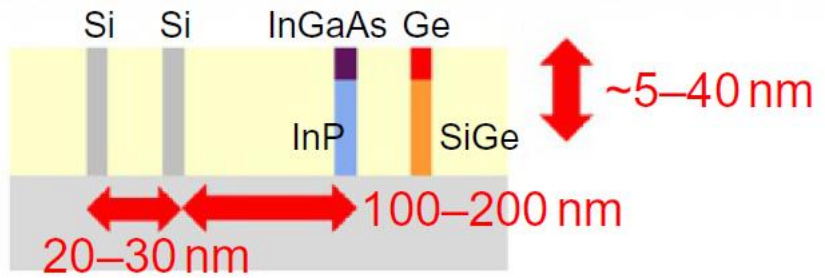
Heterogeneous Material Integration on Si Platforms

- **Growing need to integrate more functionality into a smaller form factor with power-performance benefits**

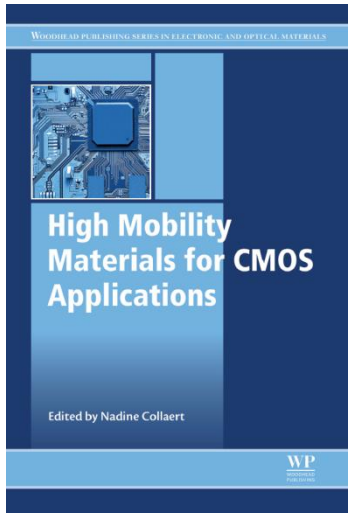
- **Need for disruptive solutions to solve Si CMOS scaling limitations**
  → **new on-chip functionalities** (sensors, high-speed I/O, optoelectronics, power management, RF)

- **Complex electronic system are still fabricated using a wide range (mix) of technologies** (Mixed-signal integrated circuit - e.g. in telecommunications)

- **Pressure to integrate heterogeneous components for performance, power and cost improvement**
  → **Beyond multichip modules & system in package**
  → **on-chip & on-die integration**



→ **Co-integration at the material level**
(in a compact volume)



High Mobility Materials for CMOS Applications.
https://doi.org/10.1016/B978-0-08-102061-6.00001-X

Heterogeneous Material Integration on Si Platforms

- **Growing need to integrate more functionality into a smaller form factor with power-performance benefits**
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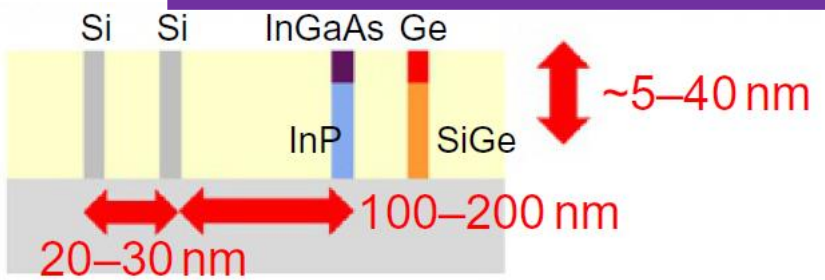
- **Cor** (Mix **logies**
- **Pre imp st**

Compatibility with large-scale 300 mm CMOS processes

Epitaxial techniques/processes adapted to:

- **Defect**
- **Stress**
- **Thermal budget**

} **management**



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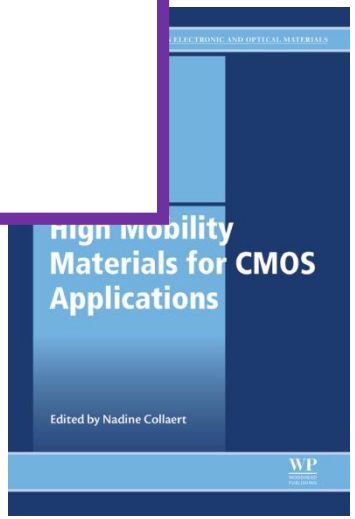

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Heterogeneous Material Integration on Si Platforms

- **Integrate** (onto Si) **heterogeneous devices with CMOS transistors**
  → **introduction of materials with specific properties**

- **Semiconductor materials chosen for their specific properties (E_g, μ)**

  e.g. InP, InGaAs, GaAs and GaN developed for mixed-signal analog RF applications

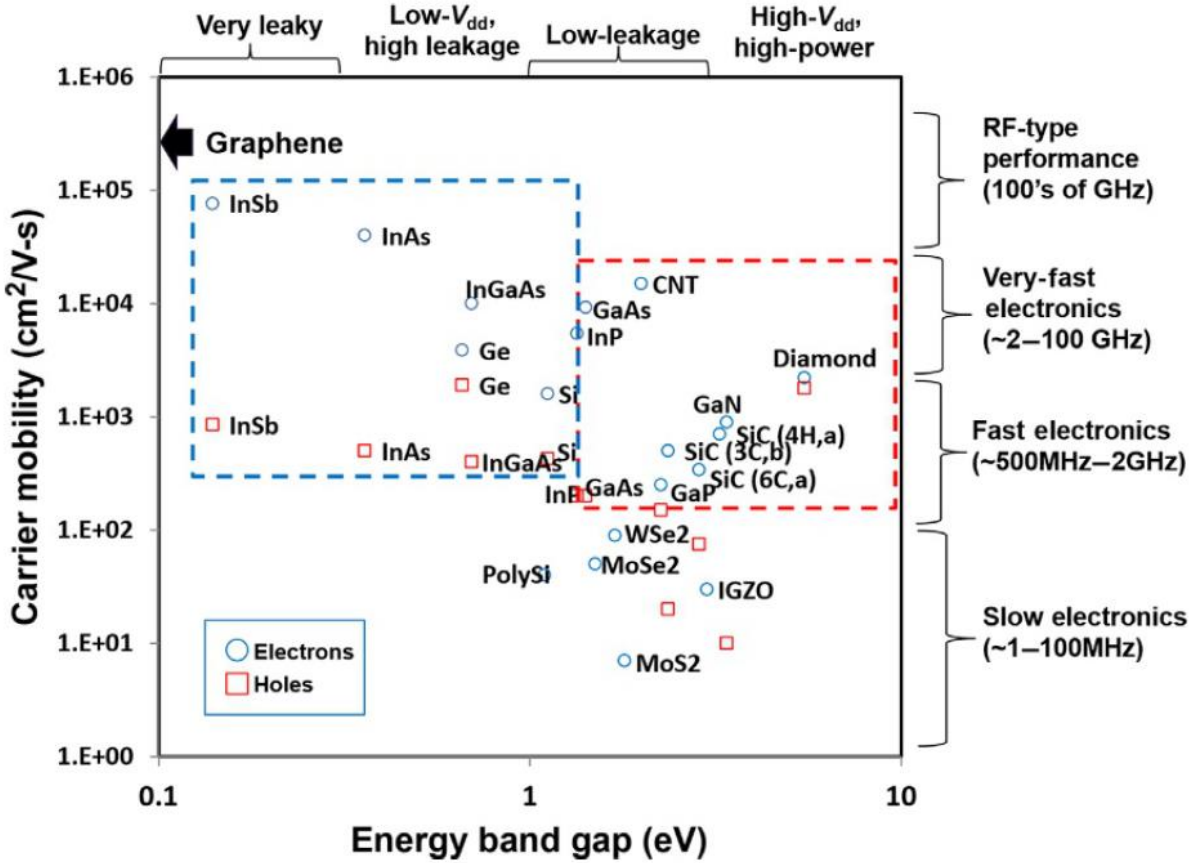

FIG. 2.8 Comparison of electron/hole carrier mobilities and energy bandgaps of selected semiconductors. *Red* box: these are some materials capable of low-leakage and high-voltage operations with switching speeds suitable for fast electronics. *Blue* box: lower bandgap materials with potential for significantly faster than silicon switching, low-voltage operations, and wide-spectrum optoelectronic response.

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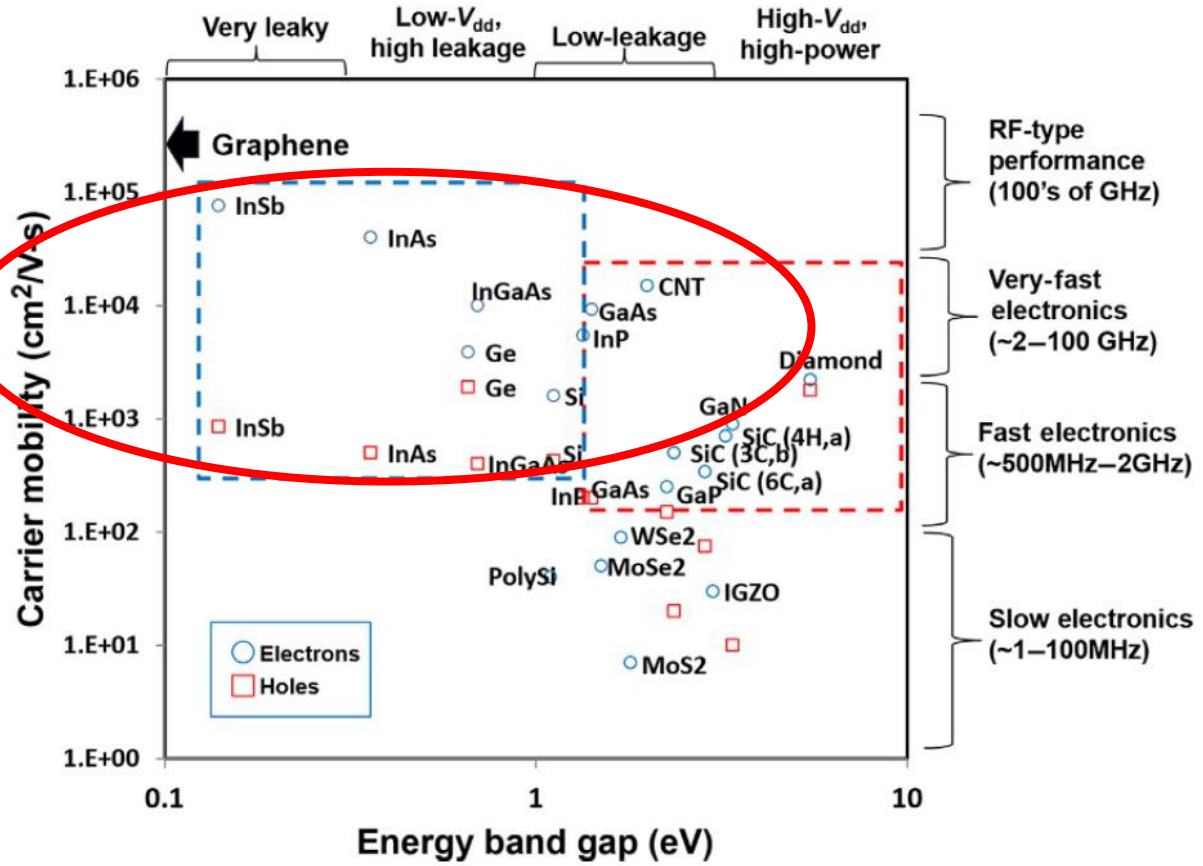
Replacement of the Si channel of the MOSFET

- **Use of strained Si**
- **Use of SiGe technology**
- **Use of a III-V material**

} **characterized by a higher mobility**



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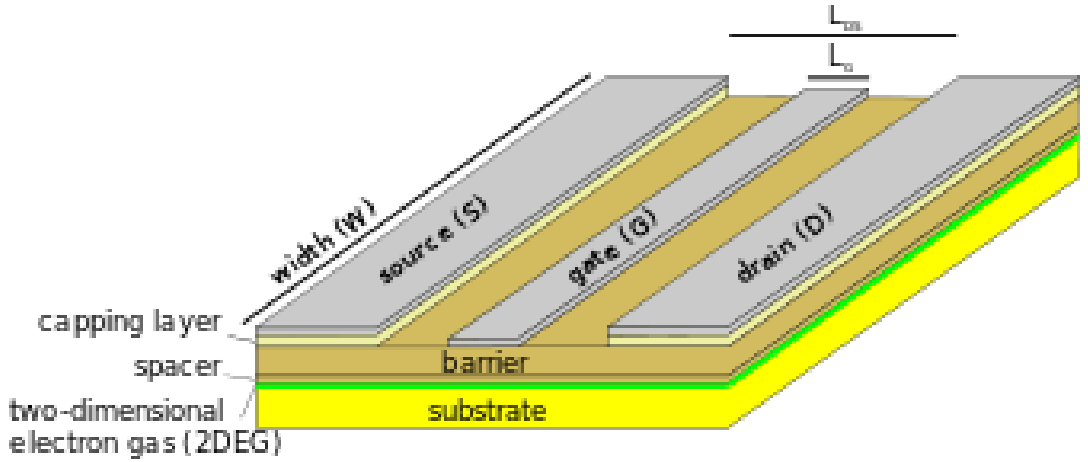
High Electron Mobility Transistor

- **A high-electron-mobility transistor (HEMT)** is a FET incorporating a **heterojunction between two materials with different band gaps as the channel instead of a doped region** (which is generally the case for a MOSFET)**.**

- **HEMTs are used in integrated circuits as digital on-off switches & as amplifiers.** They are able to operate at higher frequencies than ordinary transistors, up to millimeter wave frequencies (30-300 GHz).

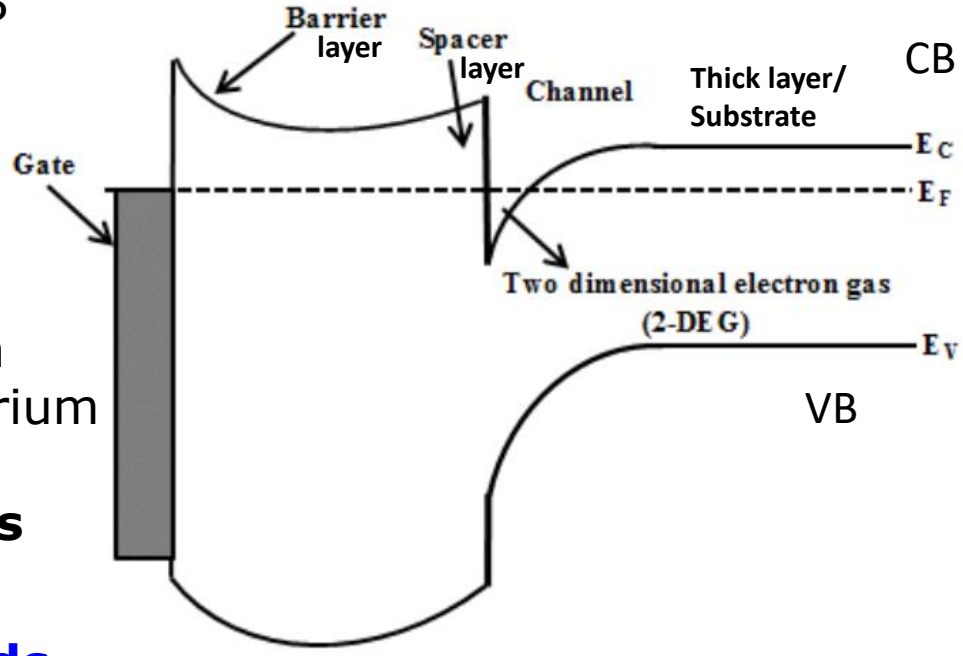
- **Applications: high-frequency products** such as cell phones, satellite television receivers, voltage converters, and radar equipment. They are widely used in satellite receivers, in low power amplifiers and in the defense industry.



https://en.wikipedia.org/wiki/High-electron-mobility_transistor

High Electron Mobility Transistor

- **The HEMT high carrier mobility and switching speed come from its specific design:**
- The wide band element (= barrier) is typically doped with donor atoms and has excess e- in its conduction band.
  These e- will diffuse to the adjacent narrow band material CB due to the availability of states with lower energy.
  The movement of e- will cause a change in potential and thus an electric field between the materials.
  The electric field will push electrons back to the wide band element CB. The diffusion process continues until e- diffusion and e- drift balance each other, creating a junction at equilibrium (similar to a p-n junction).
  The undoped narrow band gap material now has excess majority charge carriers.



Supriya, Sweety. (2012). Ballistic Mobility Degradation Effect in 25 nm Single Gate HEMT.

➡ **The charge carriers are majority carriers, which yields high switching speeds.**

➡ **The low band gap SC is undoped, i.e. there are no donor atoms to cause scattering, and thus yields high mobility.**

SiGe & III-V technology

Beyond the Si Channel

- **Replacement of the Si channel in MOSFET with higher mobility (or injection velocity) materials.**
  - **Research efforts have focused on reducing the effective mass (m*)**
    - **- strained Si MOSFET technology**

- **Beyond the traditional nonsilicon channel materials:**
  - **- Ge-based materials for improving PMOS (low hole transport m*)**
  - **- III-V-based materials for improving NMOS (low electron transport m*)**
    - **$\mu \propto 1 / m^*$**

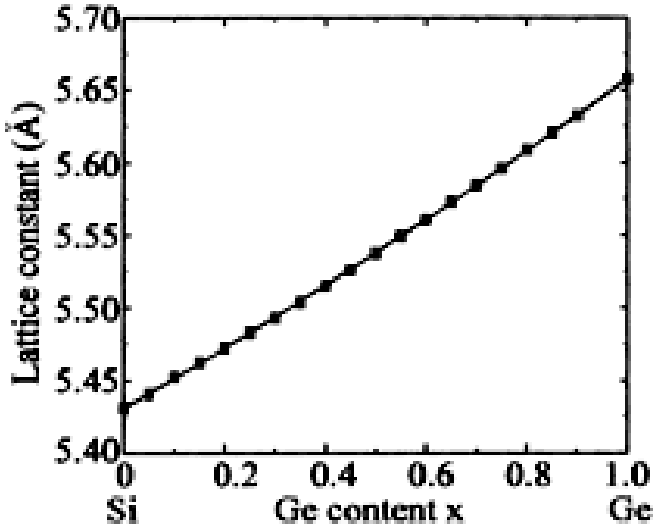
Strained Si MOSFET Technology

- **Strained Si channels have been introduced since the 90 nm node technology**
  → Use of epitaxial processes involving MOCVD or MBE growth

  ↪ higher speed operation (↗ μ) & improved current-voltage performances

- The carrier mobility increase, implemented by appropriate Si strain, provides **higher speed of the carriers** under the same conditions of polarization and a fixed oxide thickness.
  Or with the same current conditions in the channel, **thicker oxides and/or lower voltage supply can be used → relaxation of compromise between current, consumption & short channel effects**

- **Ge has a lattice constant of 5.658 Å vs. 5.431 Å for Si → up to 4.2% lattice-mismatch**



↪ **Use of an SiGe « template »** to biaxially strain Si
→ **Tensile stress = increase in the lattice parameter of strained silicon**

[Dismukes, J.P. et al., *JAP* **35** ,1964, 2899]

Strained Si MOSFET Technology

- **The strain leads to an energy splitting of the Si conduction band edge.**
- It lifts the six fold degeneracy in the conduction band and lowers the two perpendicular valleys (labeled Δ_2) with respect to the four in-plane valleys.
- **Electrons are expected to preferentially occupy the lower-energy valleys, reducing the effective in-plane transport mass.**
- **The energy splitting also suppresses inter-valley phonon-carrier scattering, increasing the electron low-field mobility.**

RIM *et al.*: DEEP SUBMICRON STRAINED-Si N-MOSFET's

IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 47, p. 1406, JULY 2000

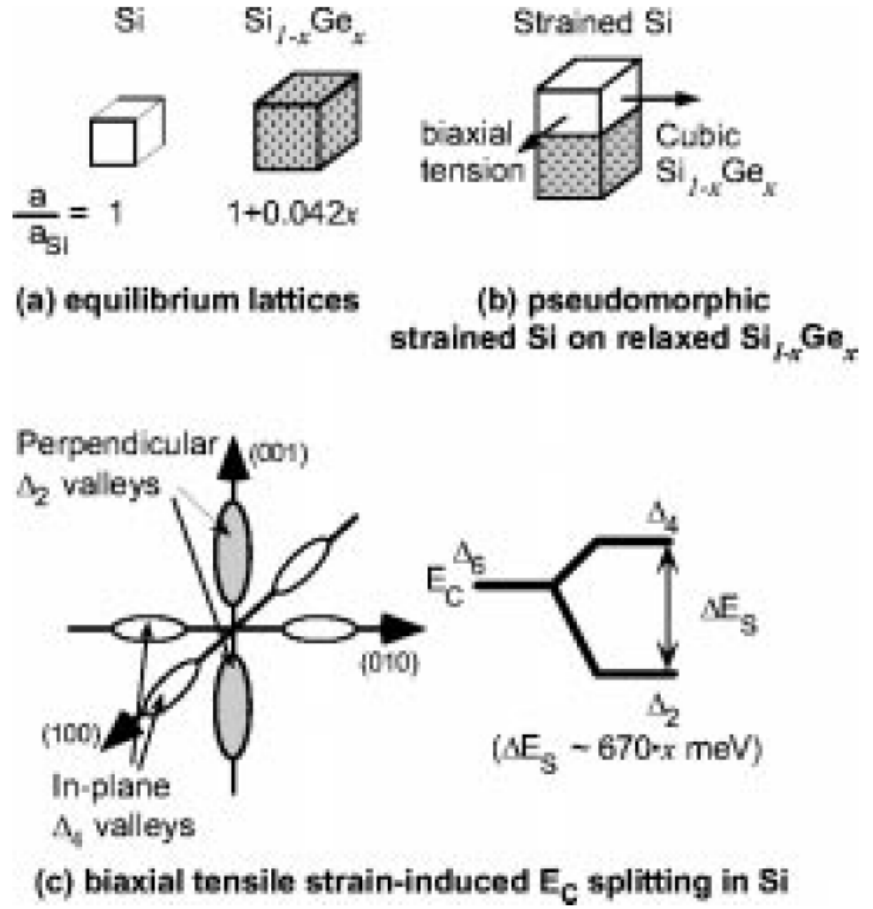


Fig. 1. Schematic illustrations of (a) equilibrium lattices, (b) peudomorphic strained Si on relaxed $Si_{1-x}Ge_x$, and (c) strain-induced conduction band splitting in Si.

Strained Si MOSFET Technology

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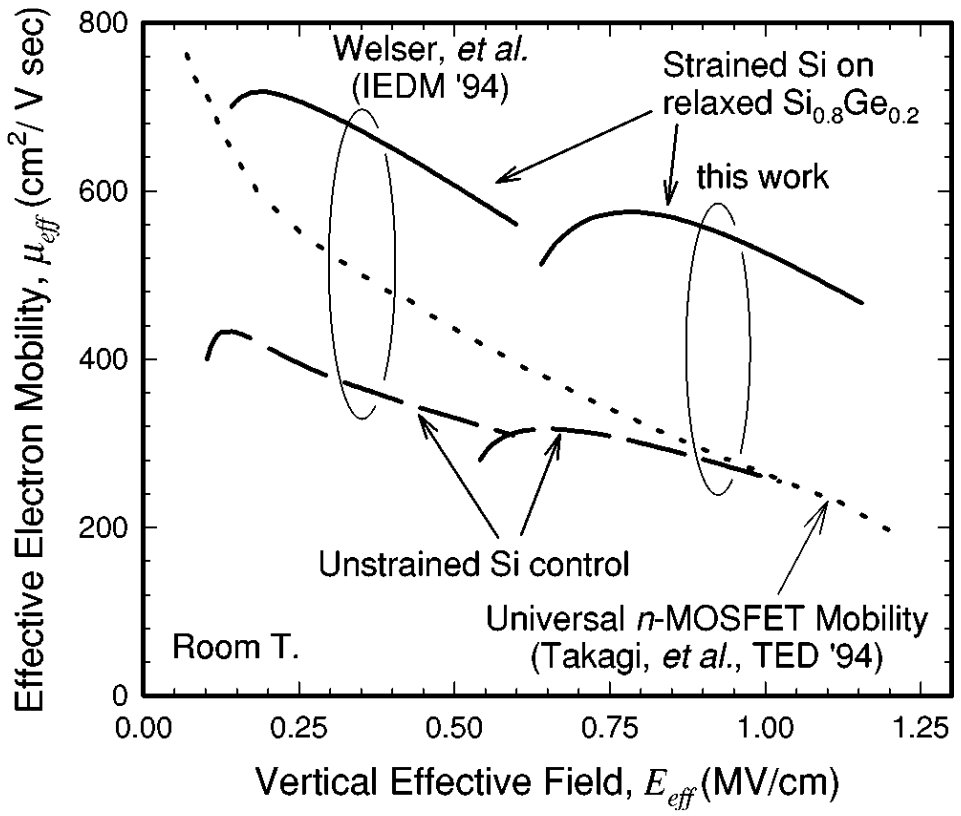

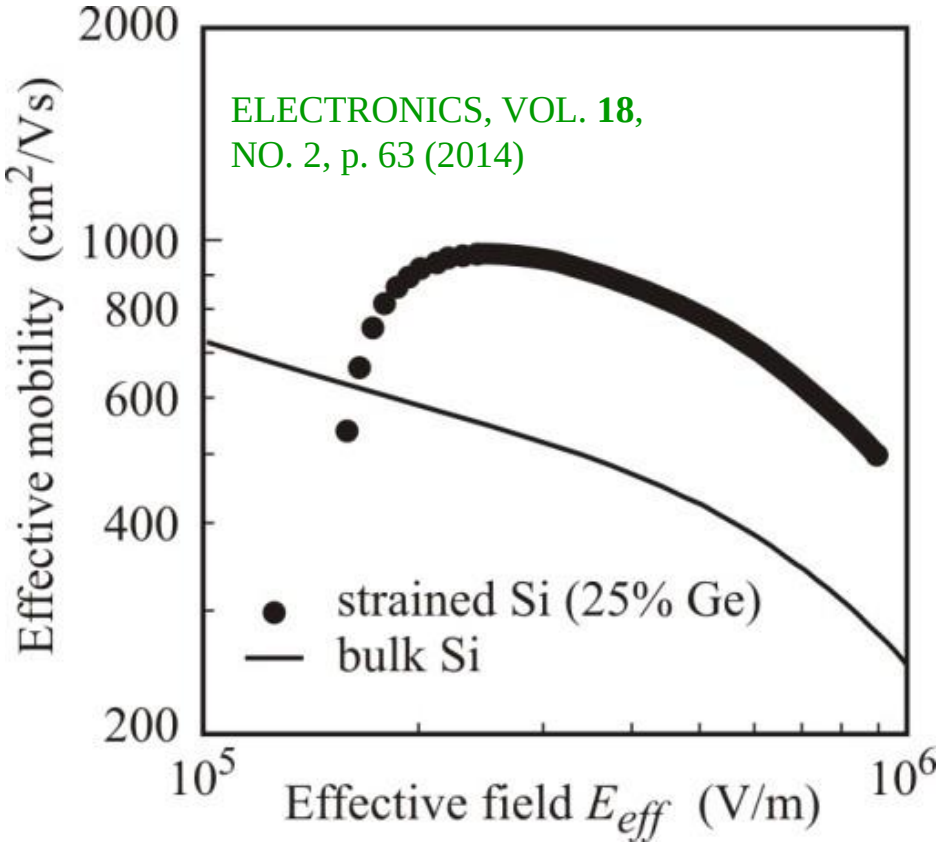

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SiGe channels

- Utilization of strained materials such as **strained Si for n-FET** and **strained SiGe for p-FET** were developed as a near-term technological solution.
- **SiGe layers pseudomorphically grown on Si substrates are under biaxial compressive strain.** SiGe layers on relaxed SiGe underlying buffers can have either biaxial compressive or tensile strain depending on the relative lattice mismatch between the two layers.

→ **Strain plays a role on the band structure and transport properties of SiGe channels**

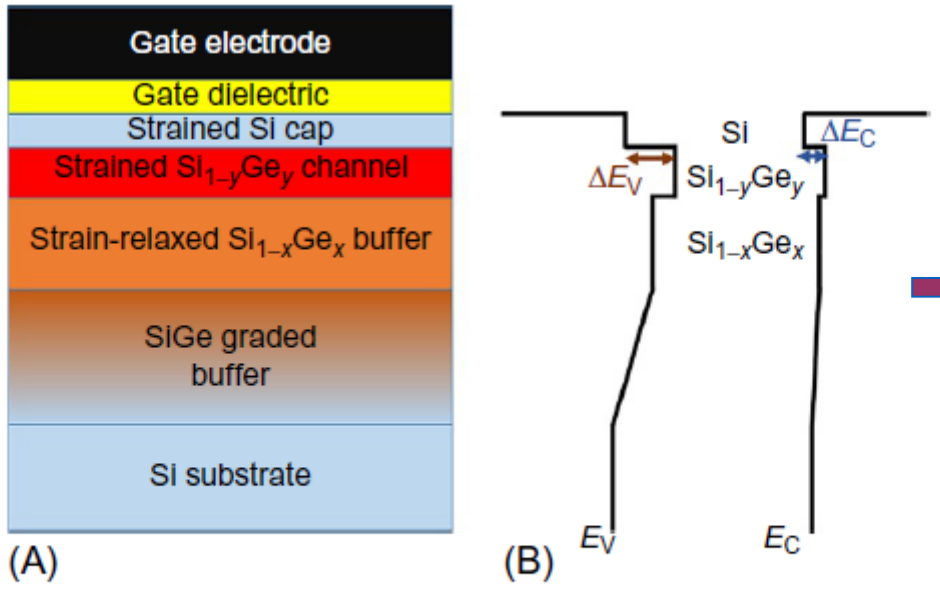

FIG. 6.1 (A) Structure and (B) band diagram of strained-Si/strained-$Si_{1-y}Ge_y$/relaxed-$Si_{1-x}Ge_x$ quantum-well heterostructure commonly used to characterize the transport in buried SiGe-channel pFETs.

- **For y > x, the buried $Si_{1-y}Ge_y$ channel layer is under biaxial compressive strain.**
- The strained-$Si_{1-y}Ge_y$ layer is capped with Si for surface passivation to control the interface traps for SiGe.

→ **The band alignment of strained Si and strained SiGe mostly confines the holes in the buried SiGe & the electrons in the strained-Si capping layer.**

Chapter 6 – SiGe Devices, Pouya Hashemi and Takashi Ando
High Mobility Materials for CMOS Applications.
https://doi.org/10.1016/B978-0-08-102061-6.00004-5

SiGe channels: Hole Transport

- **Hole mobility monotonically increases with increasing Ge content in biaxially strained-SiGe.** Adjusting the Ge content in the channel and the buffer, a wide range of mobility values can be achieved ⟹ **mobility enhancements up to 10x over (100)-Si.**
- **Moreover, extremely high hole effective mobility numbers > above 1000cm²/V.s have been measured for buried-channel strained-$Si_{1-y}Ge_y$ quantum wells.**

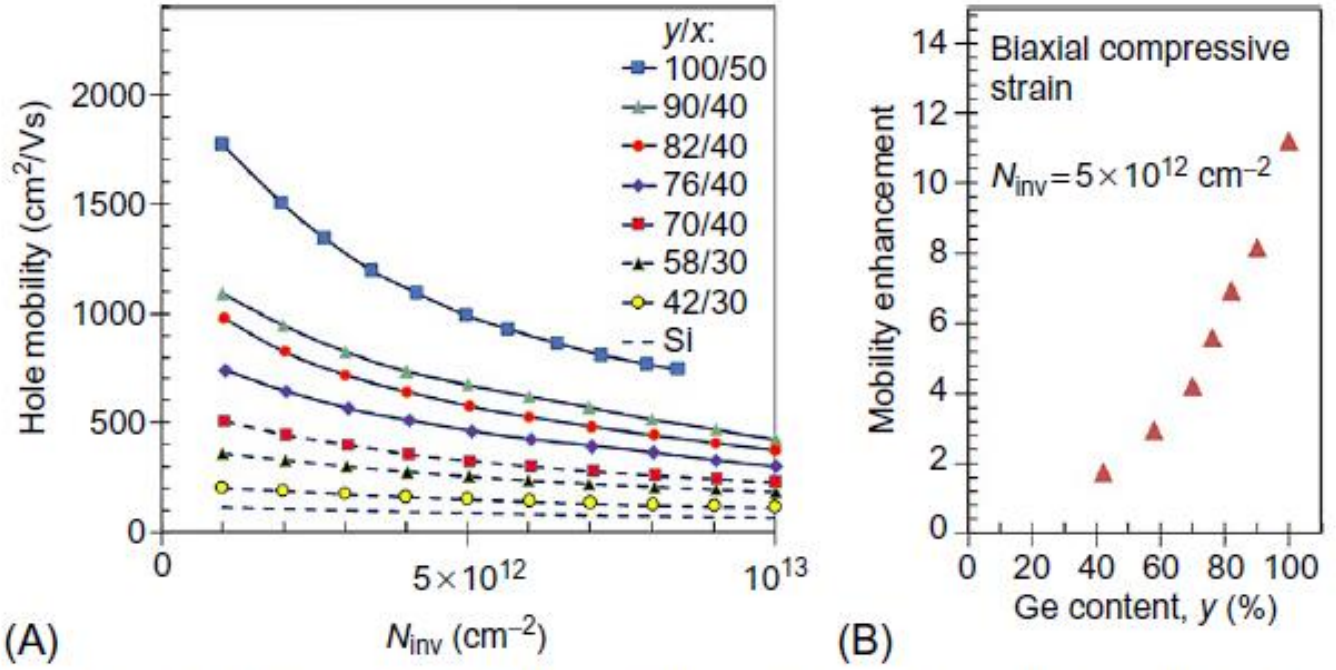

FIG. 6.2 (A) Measured effective hole mobility versus N_{inv} for strained-Si/strained-$Si_{1-y}Ge_y$/relaxed-$Si_{1-x}Ge_x$ quantum-well heterostructures for various y/x. (B) Hole mobility enhancement factor over Si versus channel Ge fraction. *(Data from J.L. Hoyt and C. Ni Chleirigh, Massachusetts Institute of Technology, with permission.)*

- **Mobility is inversely proportional to the scattering rate & the effective mass.**
- The effective mass of SiGe is a strong function of Ge fraction, strain state (compression or tension), and strain type (uniaxial, biaxial, or combined).

SiGe channels: Hole Transport

- The biaxial strain is shown to lift the degeneracy of the heavy-hole and light-hole subbands in the valence band, in addition to the effective mass reduction.
- **Also, the theory suggests that the uniaxial compressive strain can further reduce the hole effective mass and is the optimum strain for the hole transport.** The calculated hole effective mass of relaxed and uniaxially strained SiGe, lattice matched to Si, for various Ge fractions and surface orientations shows that:
  - **The hole effective mass decreases with increasing Ge content and uniaxial strain.**
- **A way to achieve uniaxial strain is to start from globally biaxial strained substrates and pattern them to high-aspect-ratio fingers or bars leading to strain relaxation along one direction.**

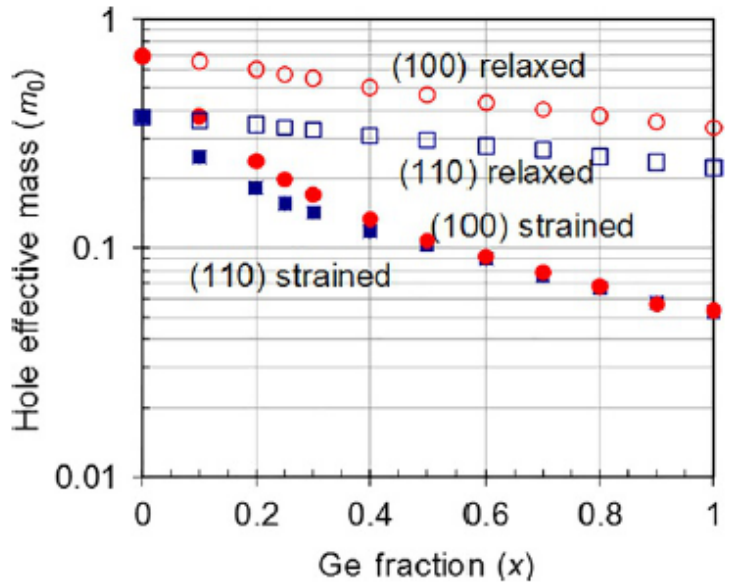

FIG. 6.3 Simulated hole effective mass as a function of Ge fraction for relaxed and uniaxial compressively strained $Si_{1-x}Ge_x$ (lattice matched to Si), with (100) and (110) surface orientations. *(Reproduced with permission from K. Ikeda, M. Ono, D. Kosemura, K. Usuda, M. Oda, Y. Kamimuta, et al., High-mobility and low-parasitic resistance characteristics in strained Ge nanowire pMOSFETs with metal source/drain structure formed by doping-free processes, in: 2012 Symposium on VLSI Technology (VLSI Technology) Digest of Technical Papers, 2012, pp. 165–166. Copyright 2012 IEEE.)*

Epitaxy Defect Engineering

Heterogeneous Material Integration on Si Platforms

- **Key challenge --> elimination of the dislocations formed when Ge or III-V materials are grown on Si.**

  → **A variety of techniques includes:**

  - **compositional grading,**
  - **wafer bonding,**
  - **selective area growth,**
  - **aspect ratio trapping,**
  - **cyclic annealing.**

[D. Caimi et al., Solid-State Electronics **185**, 108077 (2021)]

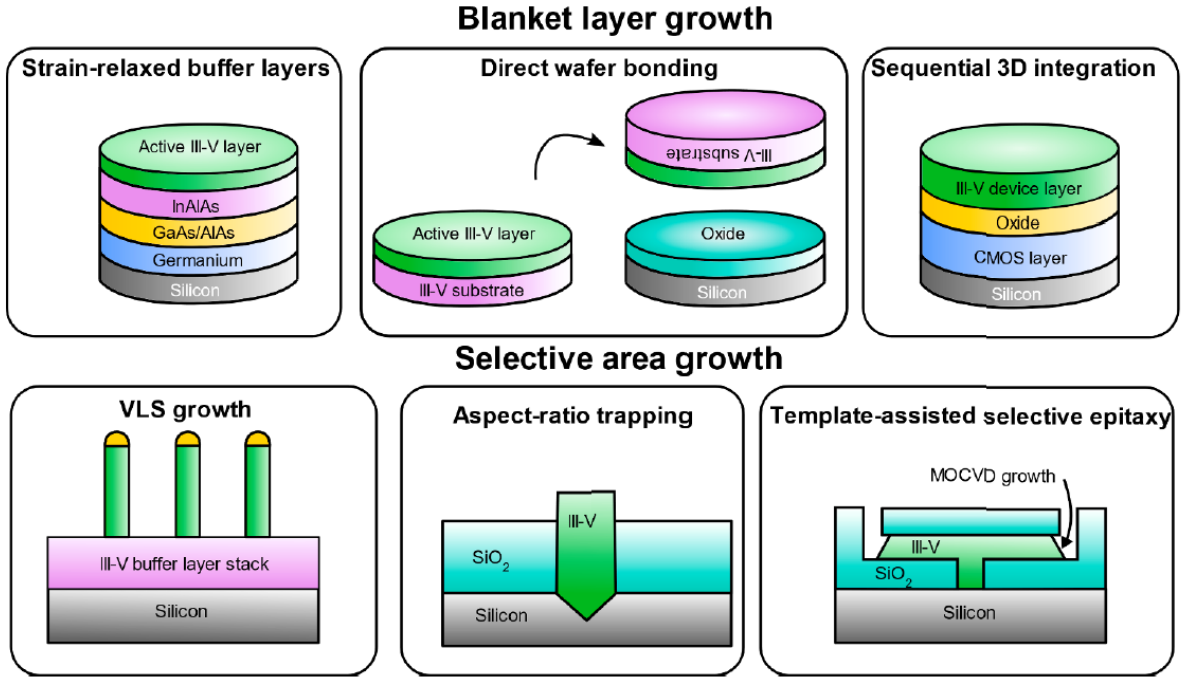

Fig. 1. Various approaches that have been explored to integrate III-V materials on Si substrates.

- **For heterogeneous devices and circuits, patterned selective-area-growth (SAG) methods provide a direct and potentially more flexible means to directly integrate disparate materials epitaxially at the fine feature level, if defectivity can be managed.**

- **Selective area epitaxy** is the local growth of epitaxial layer through a patterned amorphous dielectric mask (typically SiO_2 or Si_3N_4) deposited on a semiconductor substrate. Semiconductor growth conditions are selected to ensure epitaxial growth on the exposed substrate, but not on the dielectric mask.

Heterogeneous Material Integration on Si Platforms

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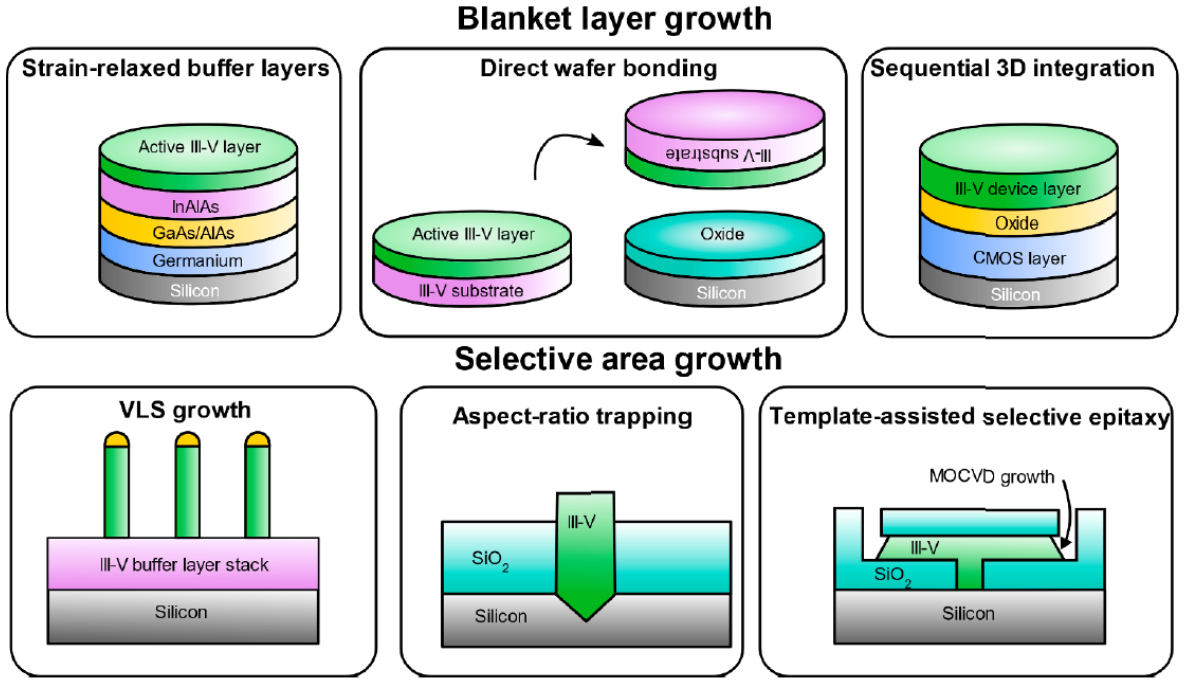

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Selective Area Growth

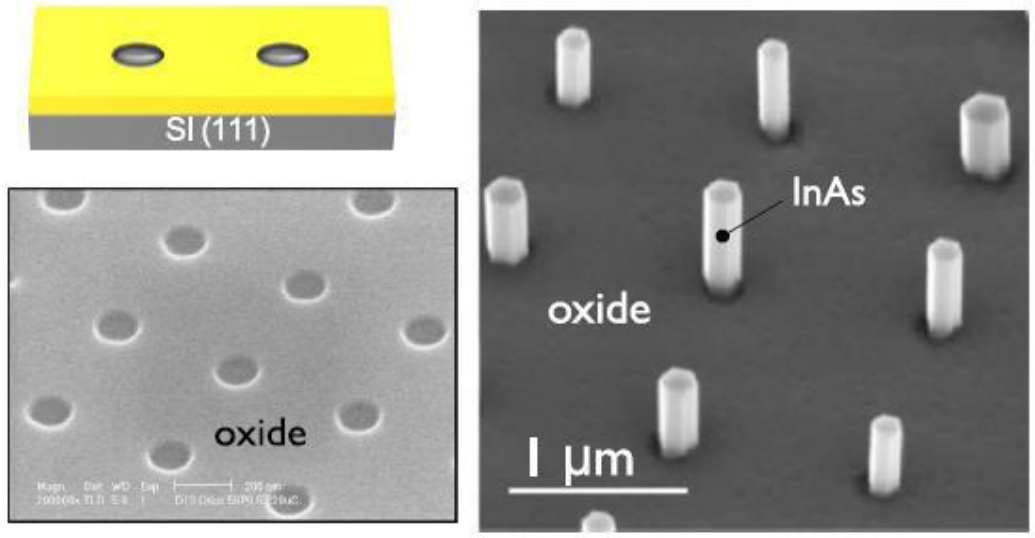
- **Selective area growth (SAG) --> local growth of an epitaxial layer on a substrate through a patterned dielectric mask** (typically silicon oxide (SiO_2) or silicon nitride (Si_3N_4)**).**

↪ **10 – 500 nm thick, covering a part of the substrate surface & leaving a defined Si surface, referred as "active area," exposed for the growth of the active layers.**

- Objective: to promote the growth of the layer only in the active area w/o nucleation on the dielectric mask.

→ exclusively in a lithography defined area, this process enables perfect alignment for the later device fabrication. But the **growth condition windows are reduced** to favour the growth rate locally.

- **Crystalline quality, process selectivity, thickness and doping control, and faceting are key properties to study and understand to enable the monolithic integration of III-V semiconductors on Si.**



[N. Collaert et al., Microelec.Eng. **132** (2015) 218]

Aspect Ratio Trapping

- **ART has been developed to integrate Ge or III-V devices with CMOS:** the buffer layer is thin (< 1 μm) to allow a standard CMOS back-end process, the technique has a low thermal budget, and the process can be applied to large wafers to allow integration into a CMOS process.
- **Ge or III-V material is epitaxially grown in high aspect ratio holes or trenches formed in dielectric layers on silicon.**

→ **In the ART technique, dislocations are guided to the dielectric sidewalls and trapped, producing a low-dislocation density region at the top of the trench.**

- **Typically, the trenches are formed in thermally-grown SiO_2 by lithography & RIE etching** (fig. 1: they are 800 nm deep, 200 nm wide and millimeters long).

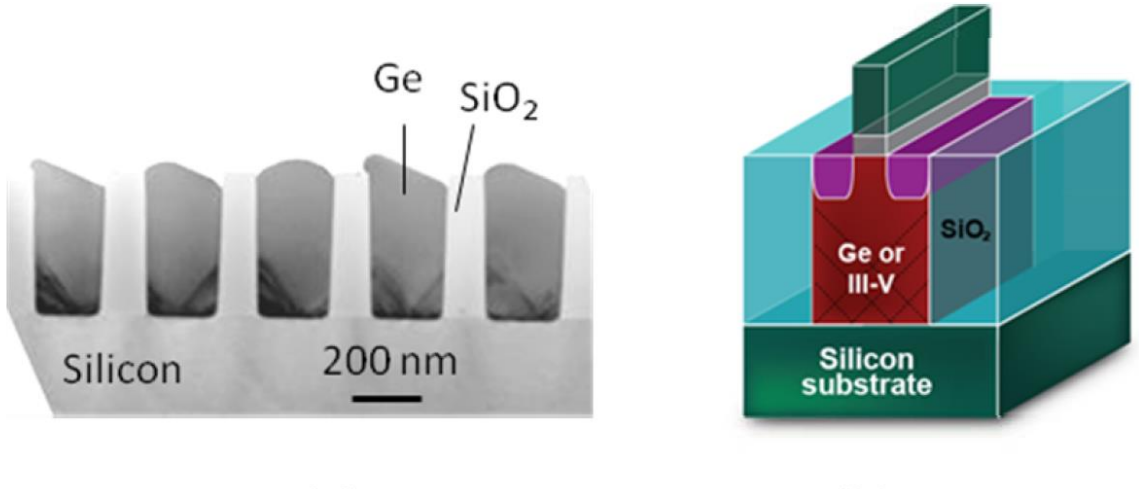


Figure 1. Depiction of Aspect Ratio Trapping using Ge in SiO_2 trenches. (a) XTEM of Ge epitaxially grown in SiO_2 trenches. Dislocations are formed at the Ge/Si interface because of the 4.2 % lattice mismatch between the Ge and silicon, but are trapped at the SiO_2 sidewall, yielding a region at the top of the trench with low dislocation density. (b) A depiction of a Ge or III-V MOSFET using ART.

[J. G. Fiorenza et al., ECS Transactions, **33** (6) 963-976 (2010)]

Aspec

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- **Ge or III-V**
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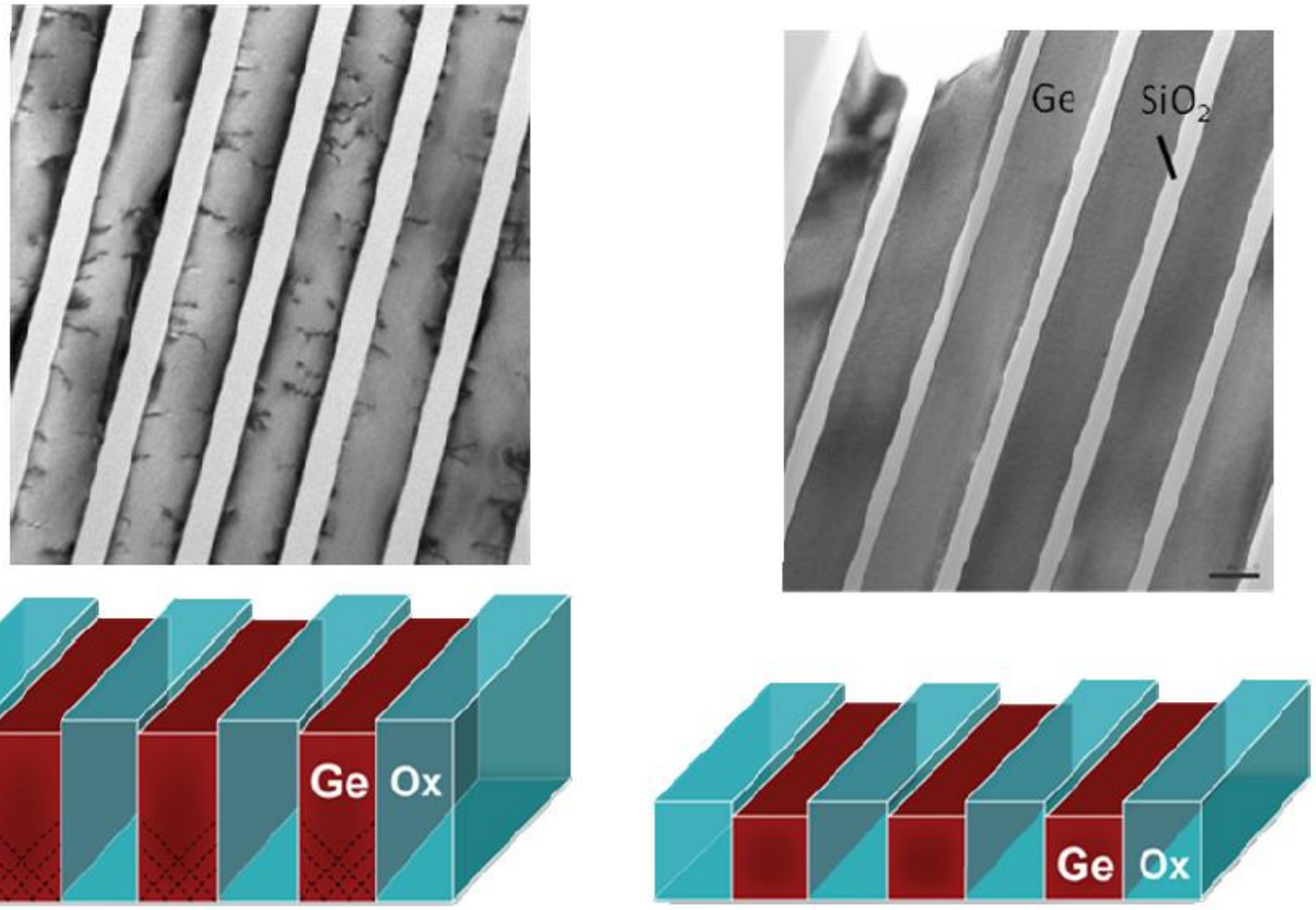

[J. G. Fiorenza et al., ECS Transactions, **33** (6) 963-976 (2010)]

Figure 2. Depiction of Aspect Ratio Trapping using Germanium in SiO_2 trenches. (a) PVTEM of Ge in trenches in a sample thinned to the bottom of the trench. (b) PVTEM of Ge in trenches in a sample thinned to near the top of the trench.

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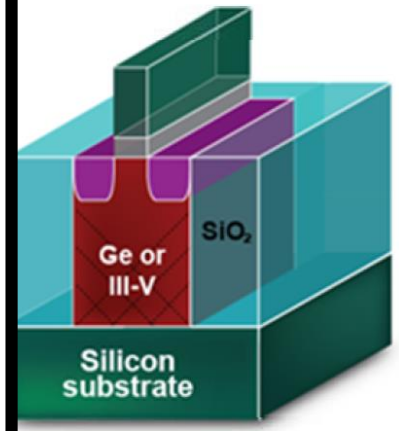


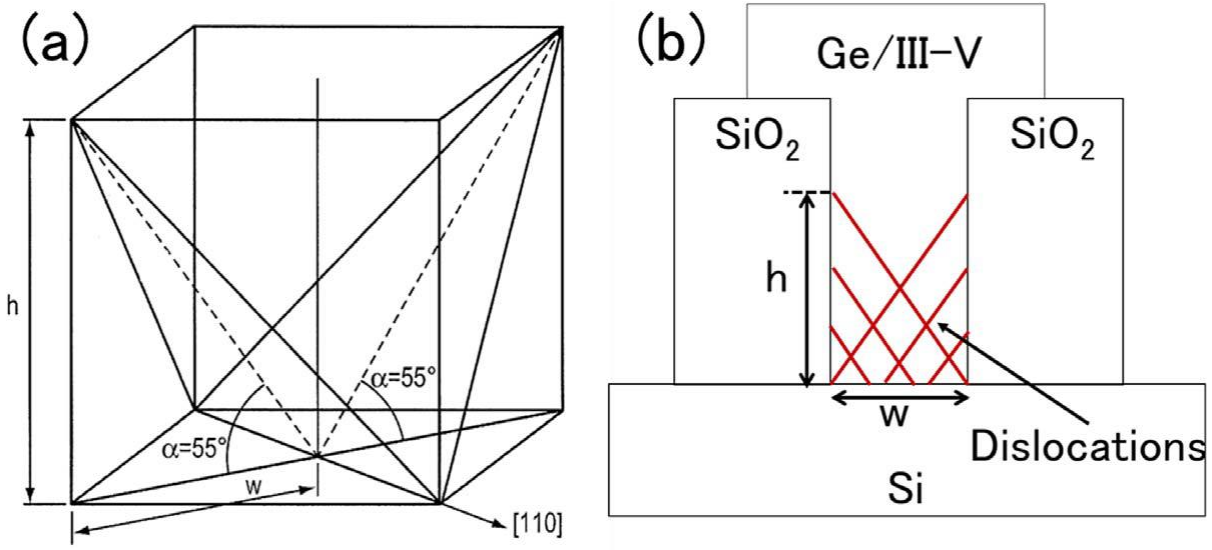
(b)

in SiO_2 trenches. (a) XTEM of
e formed at the Ge/Si interface
d silicon, but are trapped at the
ith low dislocation density. (b)

The TEM images demonstrate that the threading dislocations are eliminated in the top of the trench for a large total area of material (~5 µm²)

Aspect Ratio Trapping

- **The threading dislocations originating from the III-V/Si hetero-interface are guided to the oxide sidewalls, resulting in dislocation-free regions above a critical thickness.**
- The "trapping" of threading segments in the ART technique is attributed to the crystallographic geometry: in the {111}/<110> cubic slip system, misfit dislocations lie along the ⟨110⟩ directions in the (100) growth plane, while the threading segments rise up on the {111} planes in the ⟨110⟩ directions.



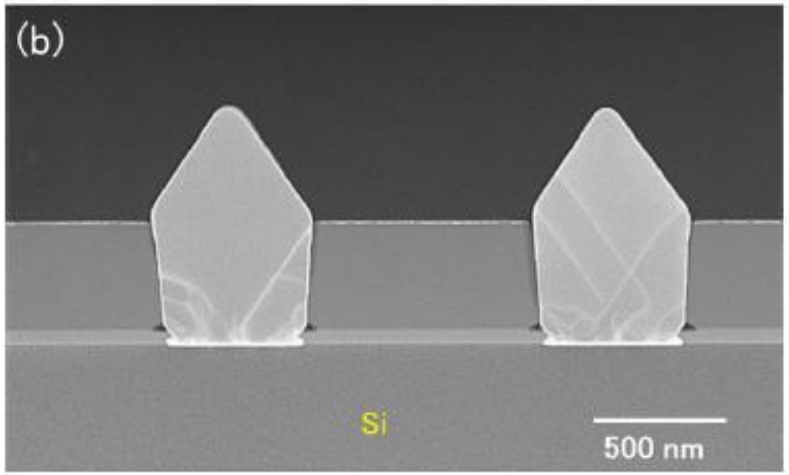


Fig. 10. (a) Tilted-view SEM image of GaAs selectively grown on a stripe patterned (001) Si substrate. (b) Cross-sectional annular dark field STEM image of GaAs-on-sub-micron-patterned-Si, showing the propagation of dislocations and stacking faults.

[Qiang Li et al., Progress in Crystal Growth & Characterization of Materials **63** (2017) 105–120]

Aspect Ratio Trapping

- ART is effective in reducing the surface TDD.

→ **The surface dislocation density is reduced by 3 orders of magnitude from blanket Ge on Si.**

- The TDD decreases proportionately with the aspect ratio (trench height/trench width)

↺ the aspect ratio itself plays an important role in the mechanism by which ART reduces the TDD.

- **ART is applicable to a variety of III-V materials (GaAs, InP).**

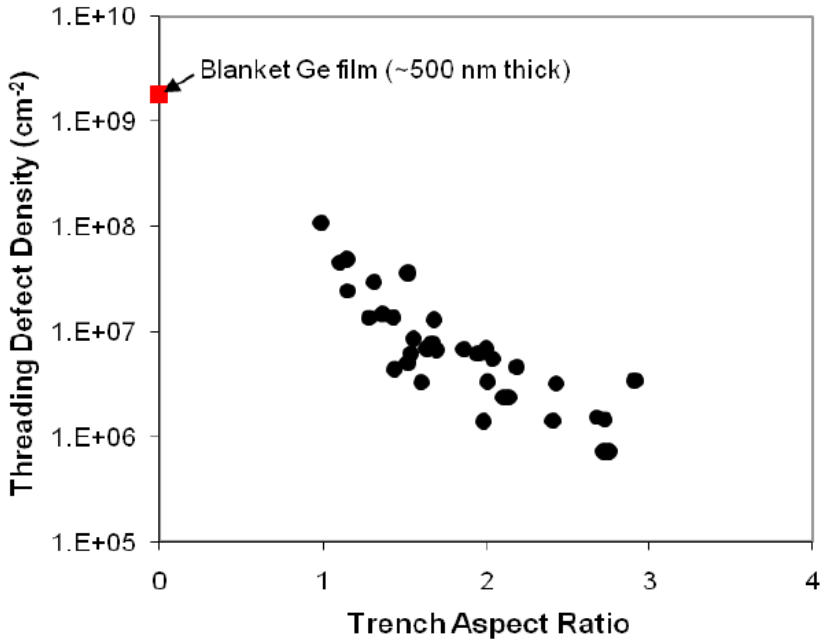
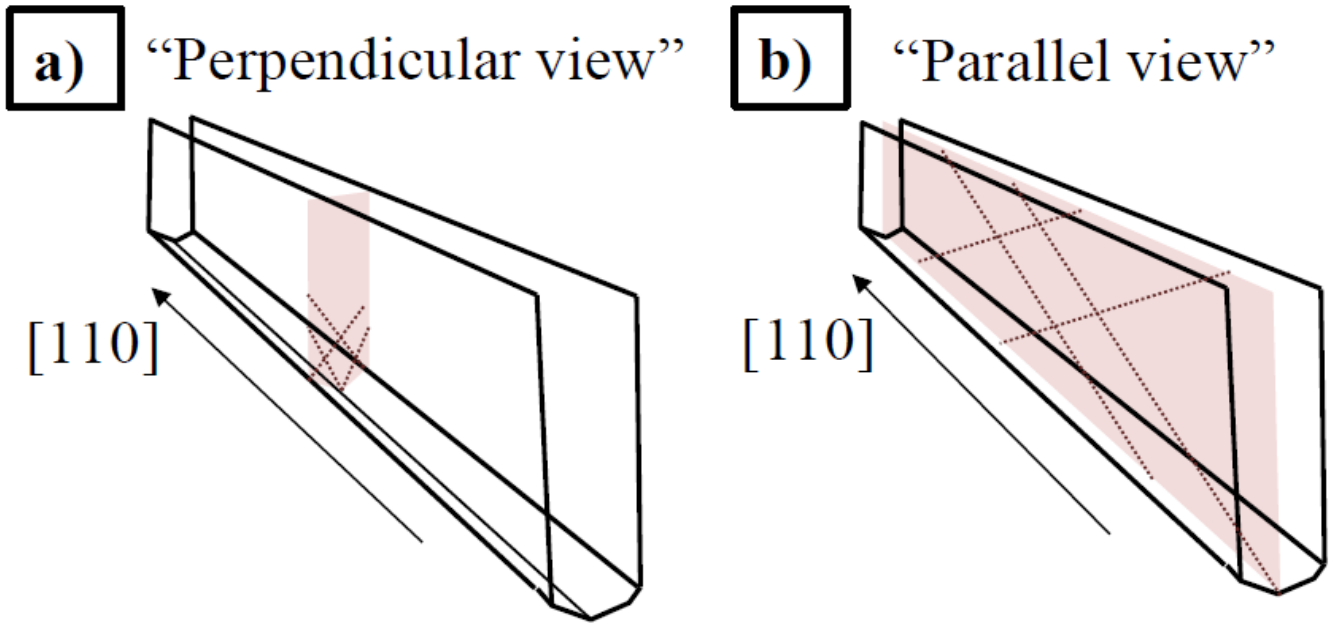


Figure 3. Threading dislocation density at the surface of a trench as a function of the trench aspect ratio.

[J. G. Fiorenza et al., ECS Transactions, **33** (6) 963-976 (2010)]

Aspect Ratio Trapping

- **Important reduction of the dislocation density within a thin deposited layer thickness** (few hundreds of nm)
- **The key challenge of this technique resides in the impossibility to trap the (111)-oriented defects along the parallel direction of the trench.**



[C. Merckling et al., ECS Transactions **66**, 107 (2015)]

Figure 1. III-V selective area growth on Si(001) in trenches. (a) ***"Perpendicular view"*** *presenting an efficient trapping effect of (111)-oriented defects from the III-V/Si interface. (b)* ***"Parallel view"*** *where (111)-oriented defects are not trapped in the direction along the trench.*

Challenges in III-V/Si Hetero-Epitaxy

- **A specific defect is antiphase-domains (APD) due to the lack of inversion symmetry of III-V materials --> the sub-lattices are occupied by different atom species. The bonds are polar due to the difference in the ionicity of the constituent atoms.**

⟹ APDs are inherent to polar-on-non-polar growth. Single layer steps produce 2 domains in the III-V overlayer whereas double-layer steps do not.

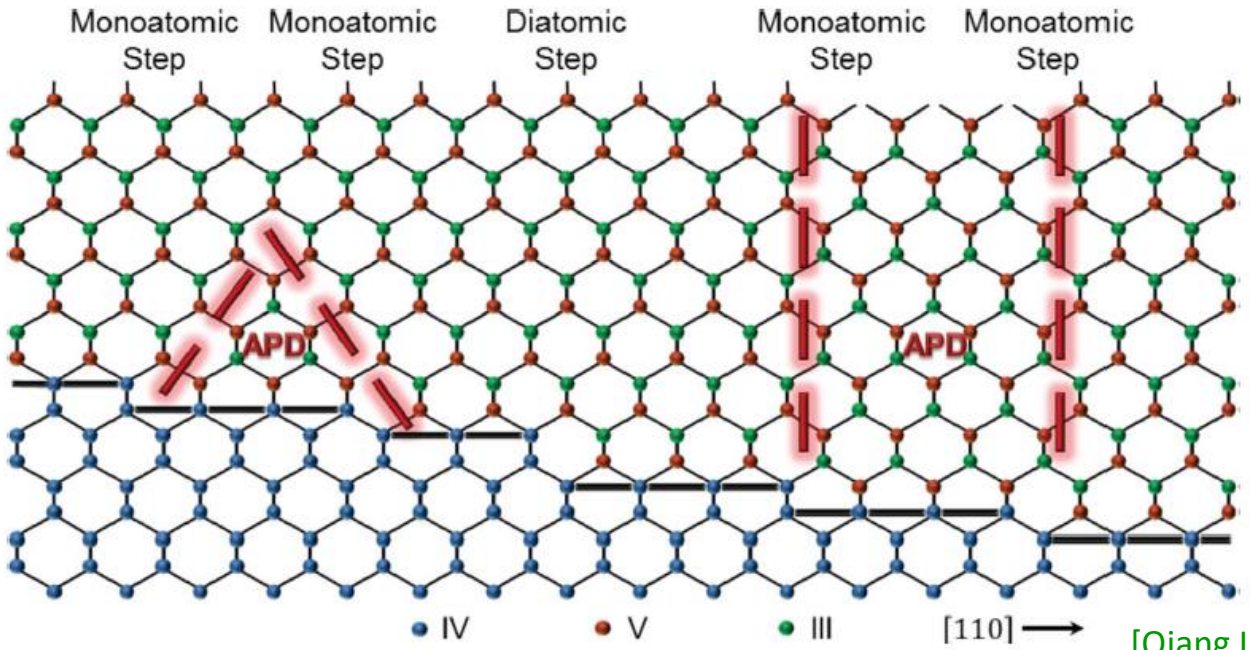
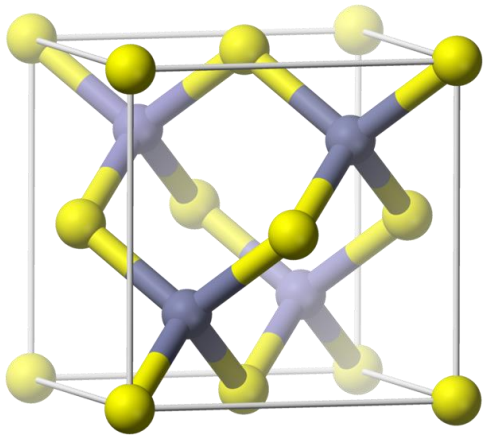
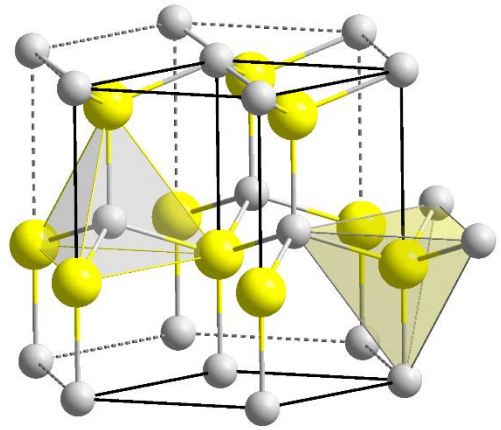


Fig. 2. Schematic down [1$\bar{1}$0], showing non-polar/polar interface between the group IV substrate and III-V epilayer. Monoatomic steps on the group IV substrate surface result in APBs, which are planes of V-V or III–III bonds. The APD can either self-annihilate (left) or rise to the surface (right). Diatomic steps on the substrate surface (center) do not result in APD formation. [27].





[Qiang Li et al., Progress in Crystal Growth & Characterization of Materials **63** (2017) 105–120]

Challenges in III-V/Si Hetero-Epitaxy

- **Development of surface preparation processes**
  → importance of the III-V/Si surface engineering to control the APD generation
  ↺ Promotion of double-layer steps at the surface

- Si (001) substrate (with a 0.15° misorientation in the [110] direction) is deoxidized in using NF_3/NH_3 remote plasma and then annealed (1 min–10 min) in an MOCVD reactor at high temperature (800 °C–950 °C) in H_2 ambient.

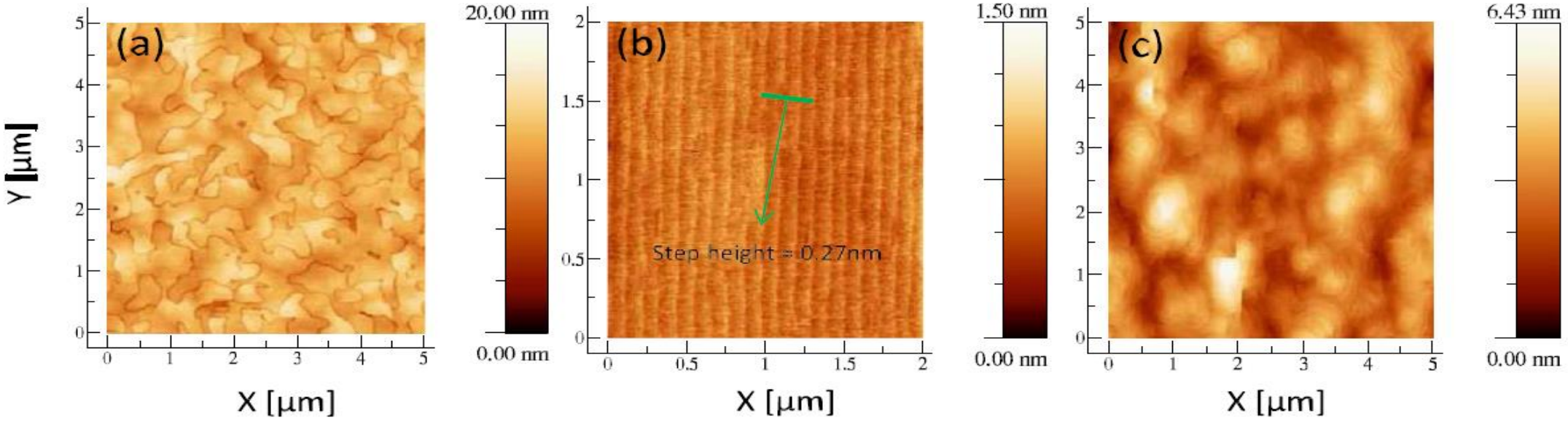


Fig. 5. (a) 5 × 5 µm² AFM image of 400 nm thick GaAs growth on un-optimized Si(001): High density of randomly oriented APBs; RMS roughness = 1.6 nm. (b) 2 × 2 µm² AFM image of 0.15° Si (001) after optimized preparation (800 °C–950 °C annealing under H_2). The surface is therefore mainly double-stepped. (c) 5 × 5 µm² AFM image of APBs-free 150 nm thick GaAs growth on optimized 0.15° Si(001): RMS roughness = 0.8 nm. [29].

[R. Alcotte et al., APL Mater. **4** (4) (2016) 046101]

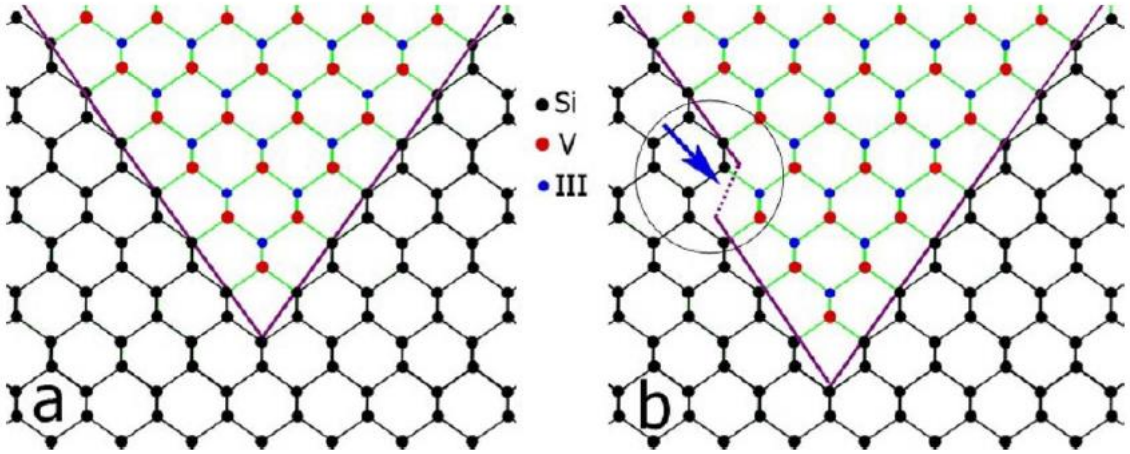
Aspect Ratio Trapping Patterned Si

- **The use of {111} Si v-grooves in the ART growth process has been developed.**

- **The crystallographic alignment between the Si and III-V materials in the V-grooves avoids the introduction of APDs.**

⟹ Crystallography analysis indicates that III-V SC on the two {111} facets of the "V-shape" have the same polarity. In principle, the Si (111) surface can also have surface steps, as in the case of Si (001) --> **A single step on the Si (111) surface has the height of one Si (111) double-layer (0.31 nm). Such steps will not lead to the formation of APDs.**

- **III-V nucleation on Si (111) generates less defects as compared to nucleation on Si (001) & avoid the formation of the (111)-oriented defects along the parallel direction of the trench.**



A III-V lattice in the V-shape of Si with {111} facets along the [110] direction.

[Qiang Li et al., Progress in Crystal Growth & Characterization of Materials **63** (2017) 105–120]

Integration of devices on a Si CMOS platform

- **From ART to epitaxial lateral overgrowth (ELO) --> formation of a continuous layer**
- **Demonstration of a GaAs MOSFET on silicon using ART.**

➡ **The transfer characteristics showed a peak mobility of 503 cm²/Vs, which was similar to the value seen on a GaAs MOSFET made on a bulk GaAs substrate using the same MOSFET fabrication process, and which exceeds the silicon universal mobility curve.**

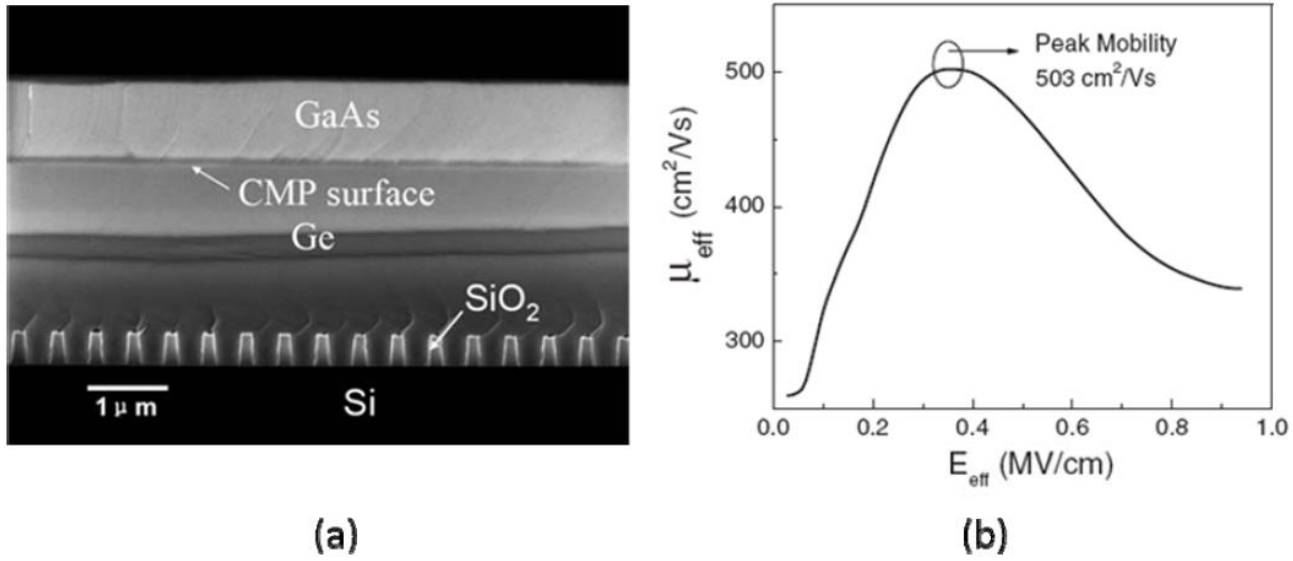


Figure 12. (a) XSEM of the epitaxial structure and (b) output characteristics of a GaAs MOSFET fabricated on silicon using ART.

[Y. Q. Wu et al., Appl. Phys. Lett. **93**, 242106 (2008)]

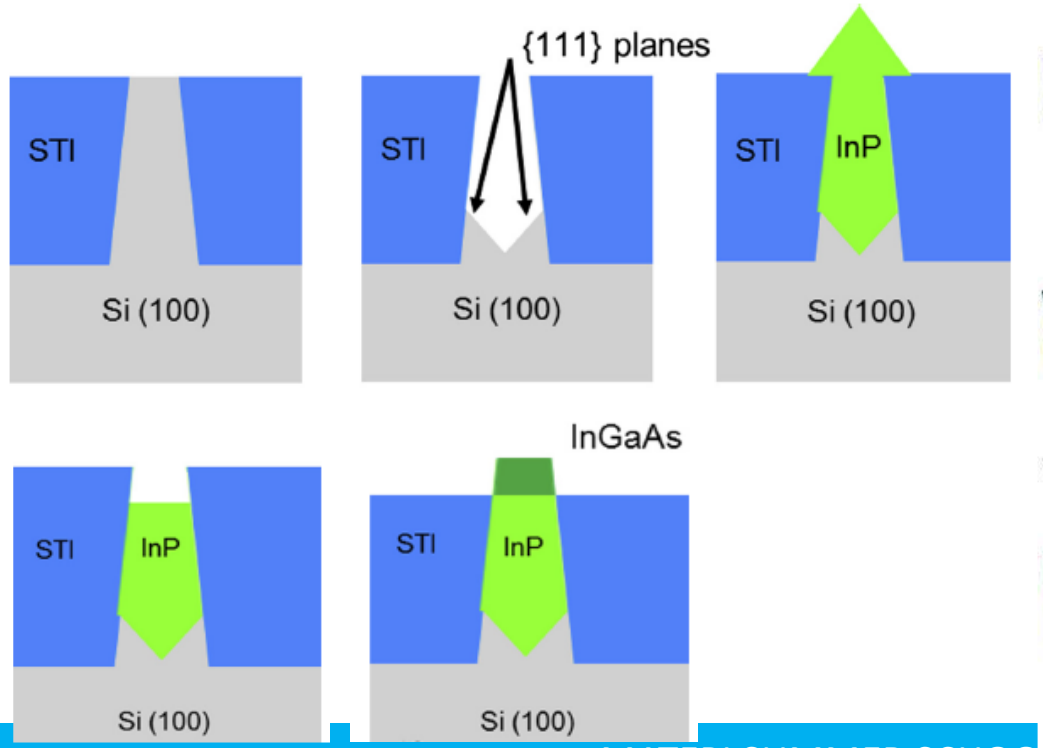
InGaAs-based channel FinFET

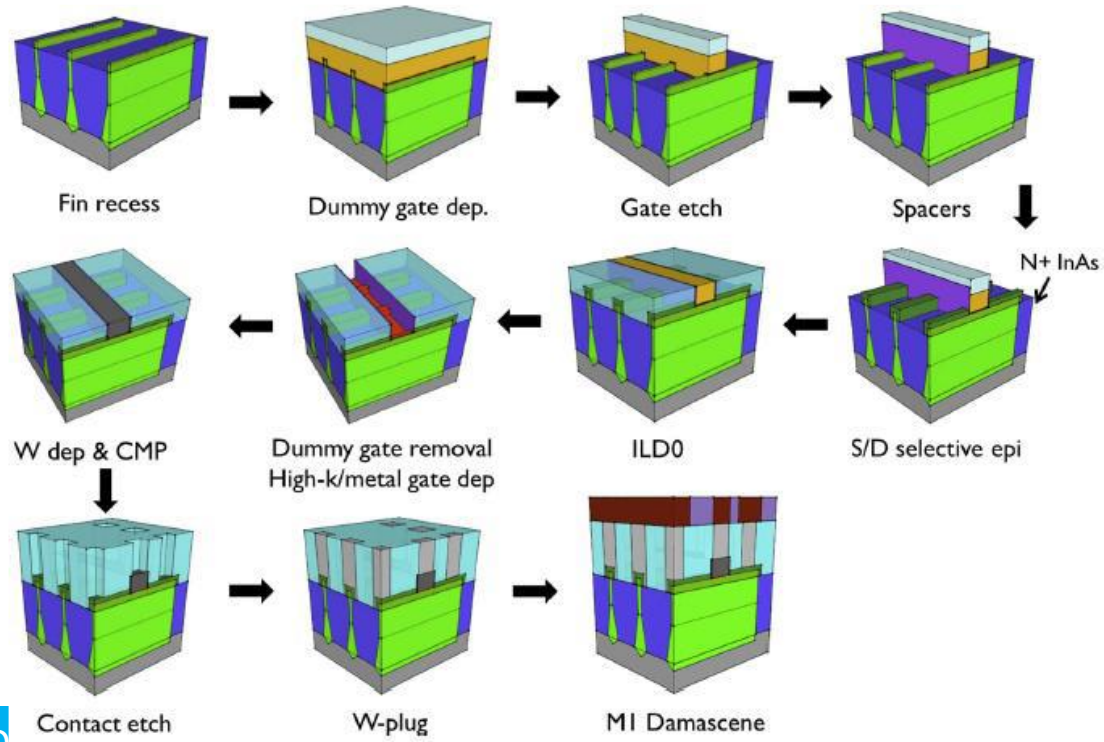
- **Initiation of the growth on the Si {111} planes and use of an InP buffer layer.**
- **Steps of chemical mechanical polishing (CMP) / chemical etching for InP recess.**

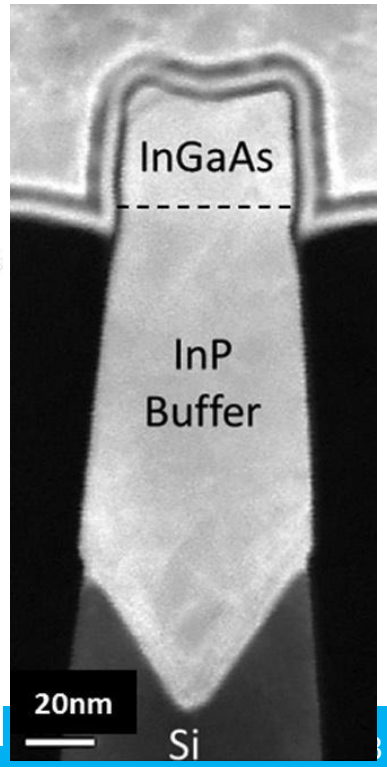
→ Growth of the $In_{0.53}Ga_{0.47}As$ channel layer --> the depth of the InP recess determines the thickness/height of the InGaAs channel.

↻ The STI oxide is recessed and then follows a typical Si Fin.

[N. Waldron et al., Solid-State Electronics **115**, 81 (2016)]



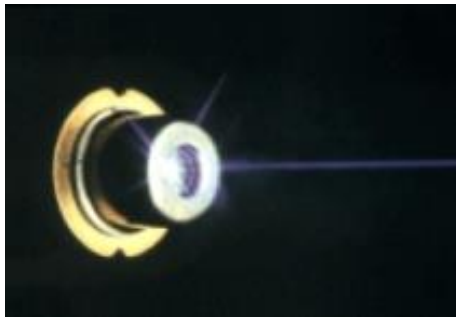




GaN Electronics

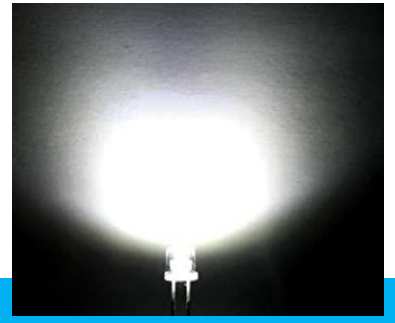
Why GaN ?

Optoelectronic Applications:

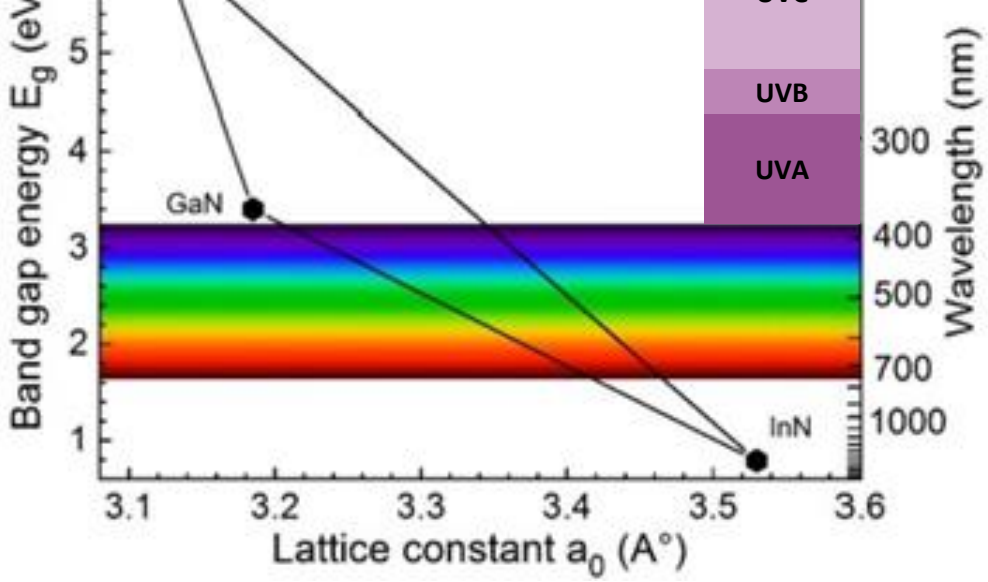


LED, lasers, …

- **Wide band Gap semiconductors (AlN, GaN)**
- **From IR to UV**
- **Wide range of applications**



→ **White light LED**



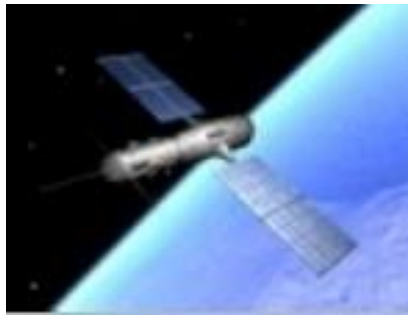
The Nobel Prize in Physics 2014

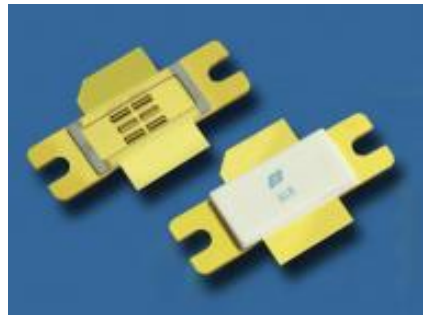
Isamu Akasaki, Hiroshi Amano, Shuji Nakamura

" For the invention of efficient blue LEDs which has enabled bright and energy-saving white light sources "

Why GaN ?

Electronic Components:





Telecommunication, radars, power electronics,…

Properties (300 K)	Si	InP	GaAs	4H-SiC	GaN
Band Gap Energy (eV)	1.12	1.35	1.43	**3.25**	**3.43**
Breakdown Field F_{cl} (MV/cm)	0.3	0.45	0.4	**3**	**3**
Electron Saturation Velocity v_s (x10^7 cm/s)	1.1	1	1	**2**	**1.8**
Thermal Conductivity Θ_K (W/cm.K)	1.5	0.7	0.5	**4.9**	**1.5**

$$\longrightarrow P_{\max} \propto I_{\max} \times V_{cl}$$

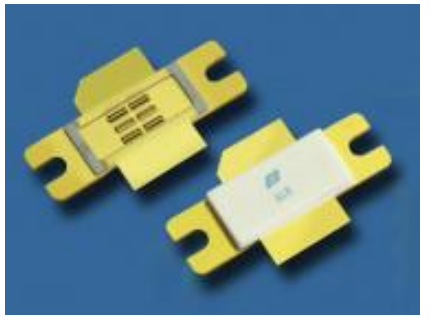
$$\longrightarrow f_c \propto v_{sat}$$

(Cutoff frequency)

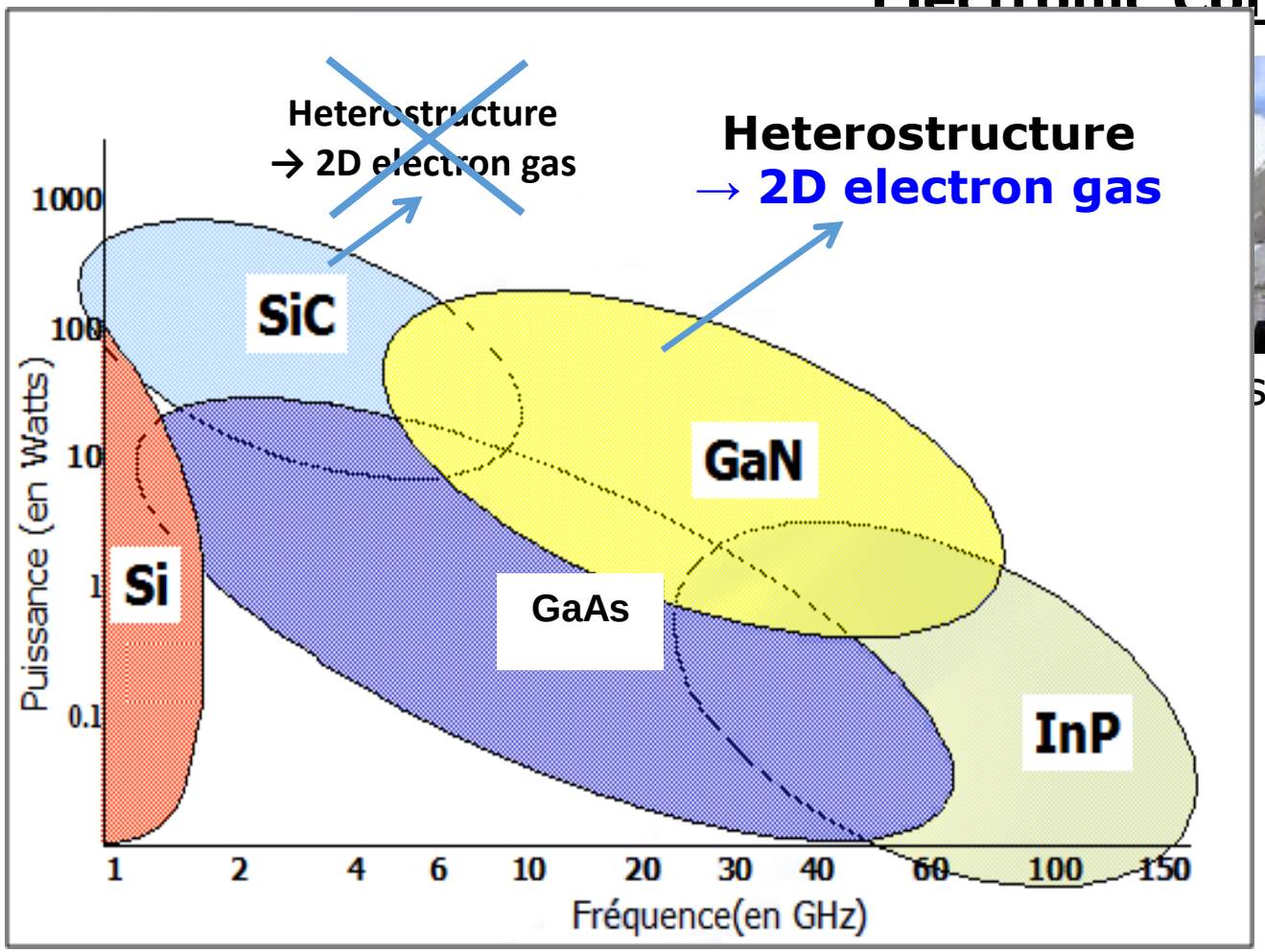
GaN --> high breakdown field, good thermal conductivity, high electron saturation velocity

Why GaN ?

Electronic Components:



s, power electronics,…

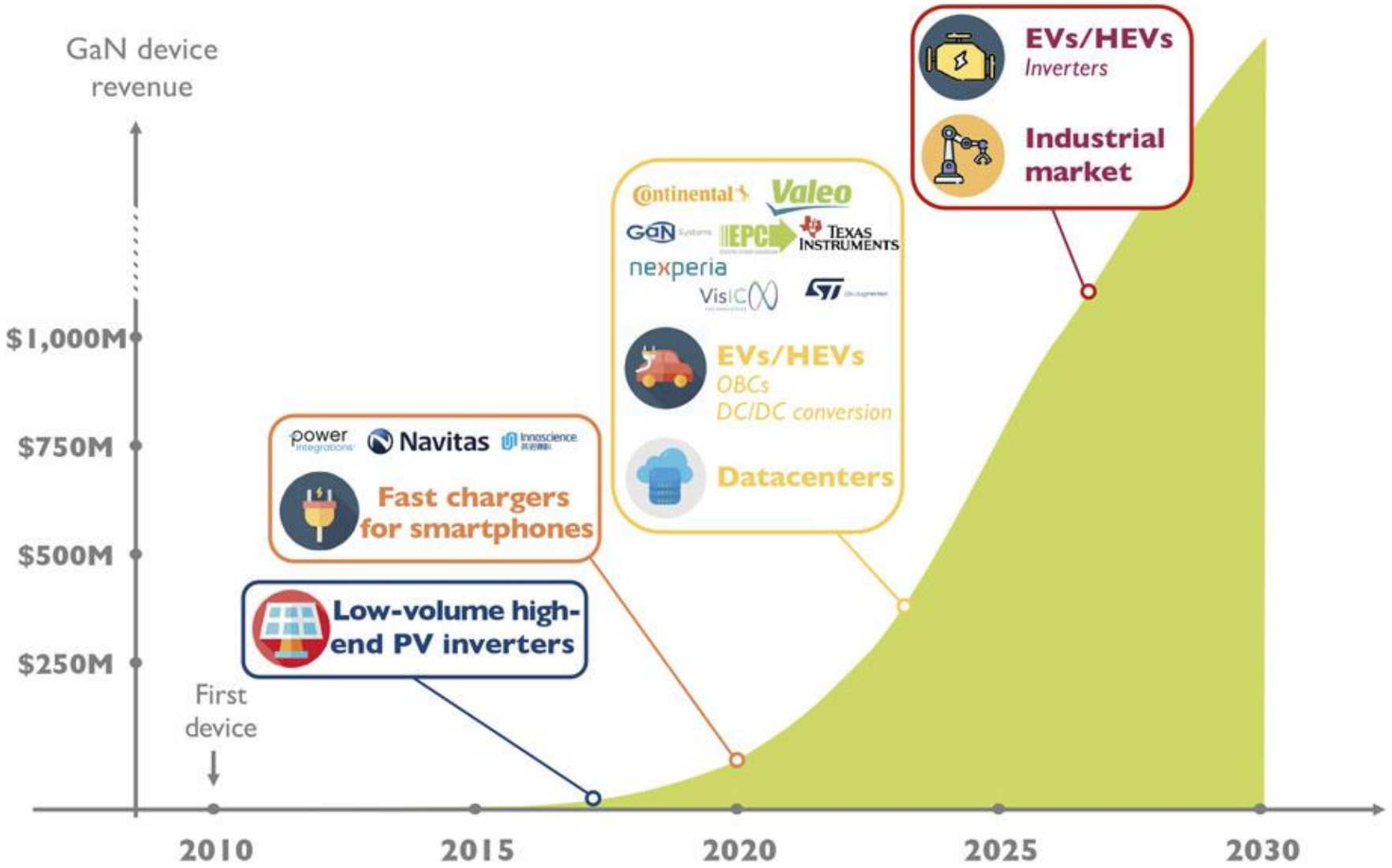


GaN: well-adapted material for high-frequency high-power electronic components

Roadmap for GaN power devices

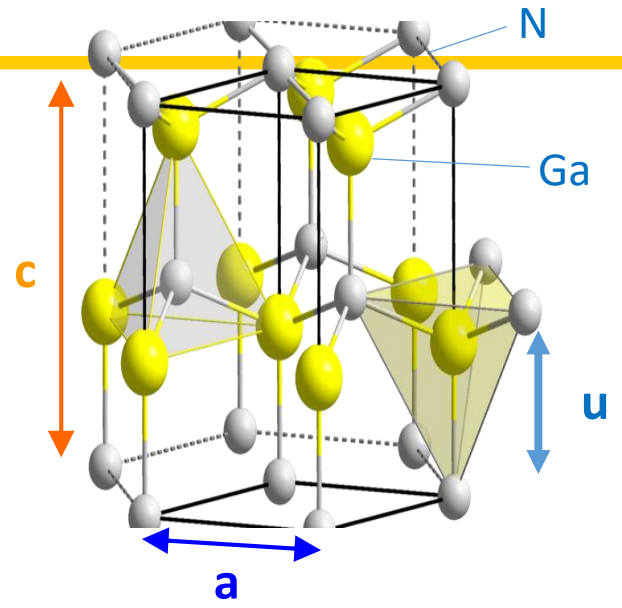
(Source: GaN Power 2021: Epitaxy, Devices, Applications and Technology Trends report, Yole Développement, 2021)

New players have entered the market with GaN-on-Si enhancement-mode (E-mode) **high-electron-mobility Transistor (HEMT) technology**



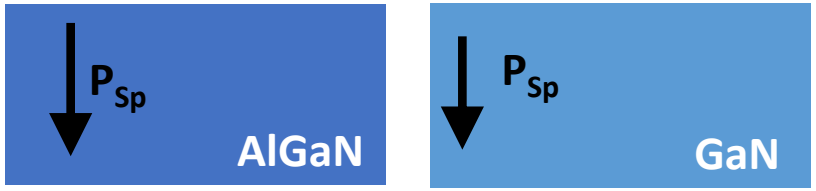
www.semiconductor-today.com/news_items/2021/may/yole-100521.shtml

GaN Crystal Structure & Polarization



- **Wurtzite structure with two hexagonal sub-lattices**
- **A unique c-polar axis**
- **Non ideal wurtzite structure**
  - **the tetrahedron is distorted**
  - **c shorter = tetrahedron compressed along c**

- **Spontaneous polarization (P_{sp})**
  - **The direction depends on the film polarity (Ga or N polar)**



(Ga, Al) polar

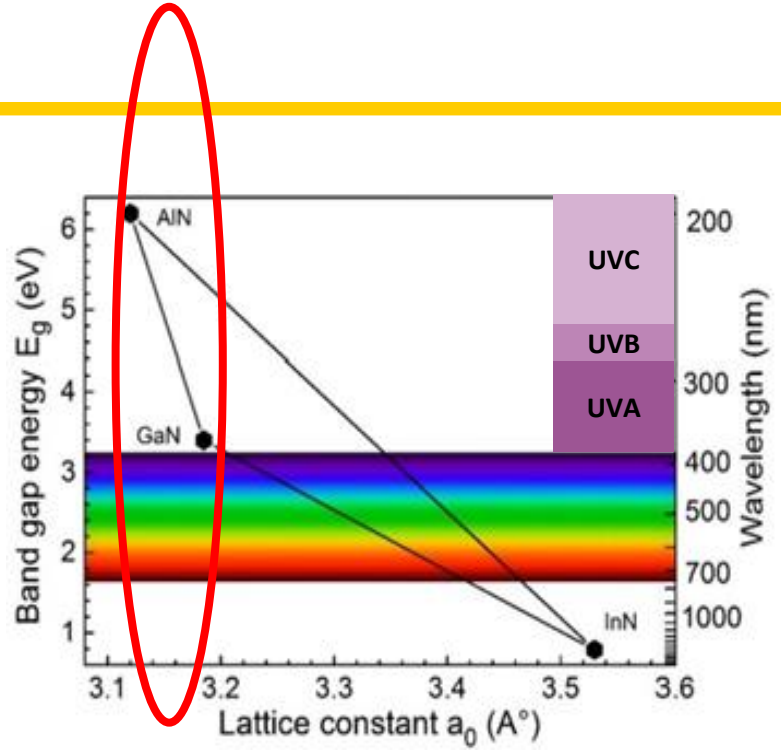
	a(nm)	c(nm)	c/a	u/c
GaN	0.3189	0.5185	1.626	0.377
AlN	0.3113	0.4982	1.600	0.382
InN	0.3538	0.5703	1.612	0.377

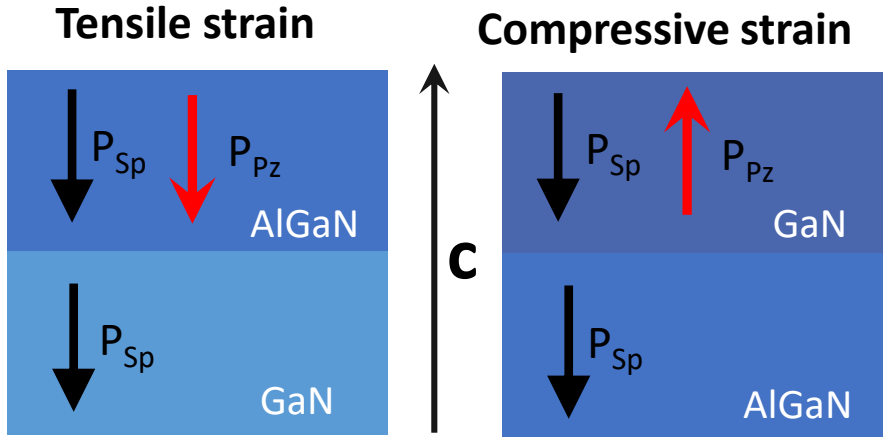
Ideal wurtzite

c/a	c/u
1.633	2.666

Polarization in Heterostructures

- **Wurtzite structure with two hexagonal sub-lattices**
- **A unique c-polar axis**
- **Piezoelectric polarization (P_{pz})**
  - **Due to the epitaxial strain (the direction depends on the type of strain)**
- **Total polarization ($P = P_{sp} + P_{pz}$)**





Polarization in a AlGaN/GaN Heterostructure

➢ **Total polarization ($P = P_{sp} + P_{pz}$)**

Heterostructure

↓

Different total polarization

↓

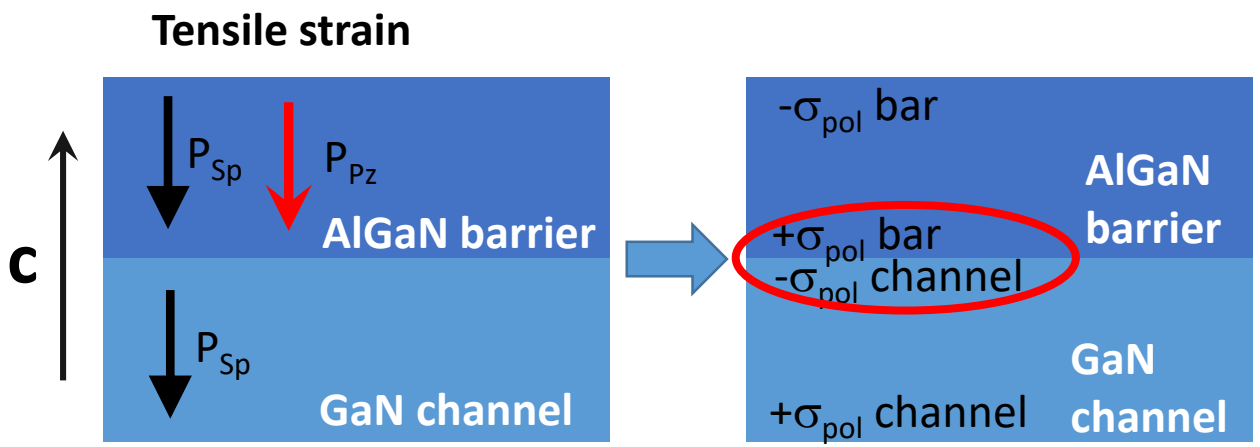
Charge densities at the interface

↓

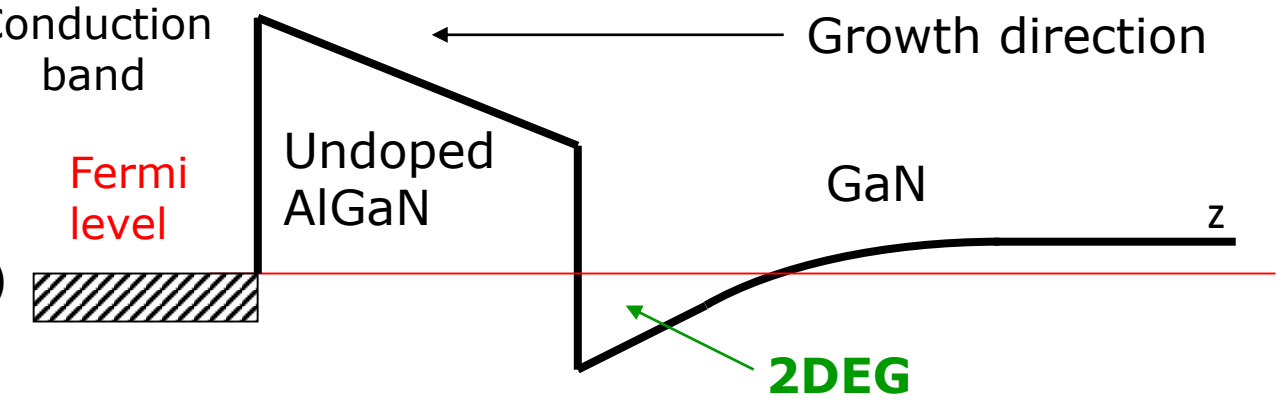
Internal electric field

↓ $F = \Delta P = (P_{bar} - P_{cha})/\varepsilon\varepsilon_0 = \sigma/\varepsilon\varepsilon_0$

Band structure bending



HEMT heterostructure:
A cladding barrier (larger gap than GaN) is grown on the GaN channel



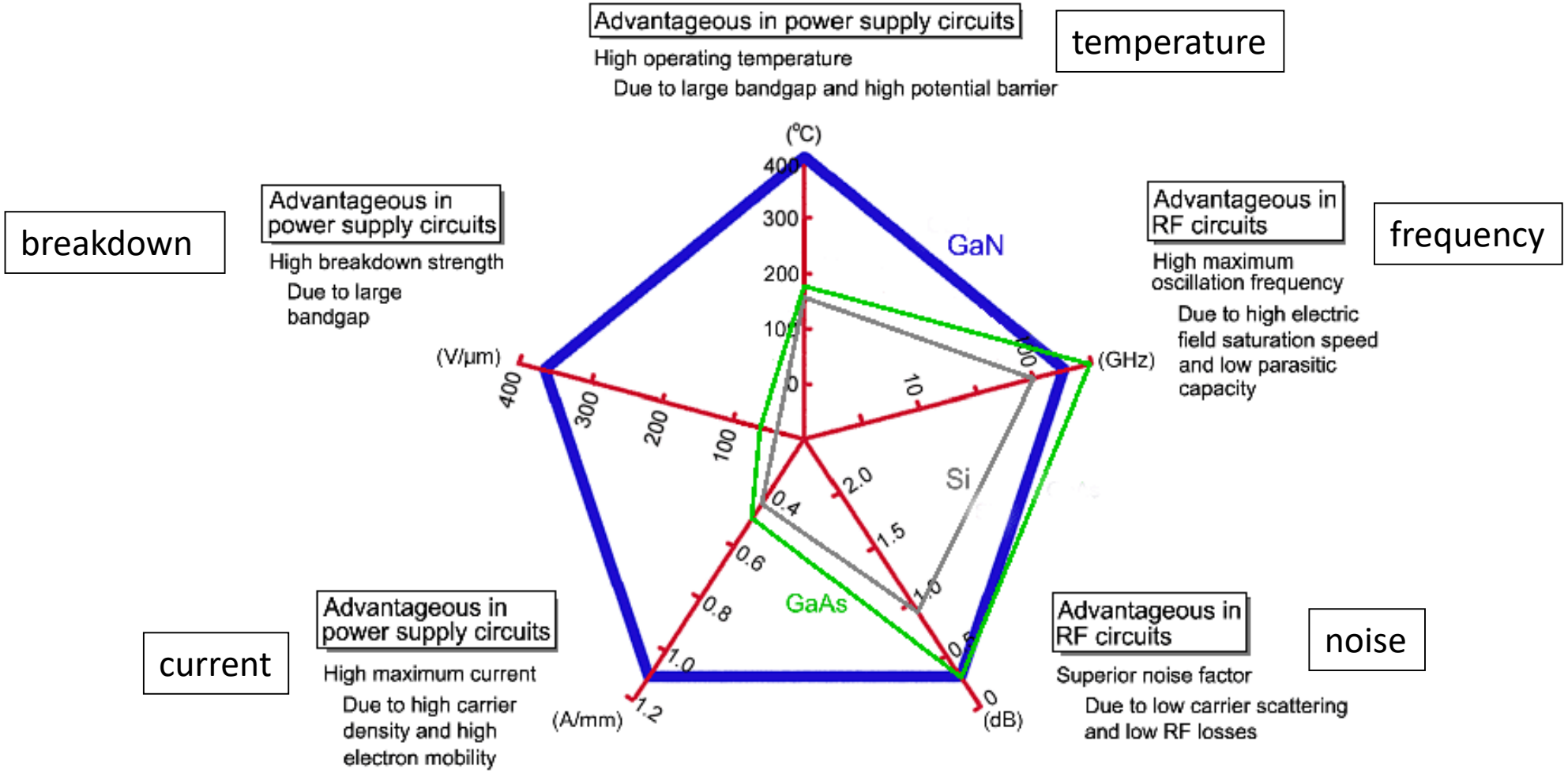
At the AlGaN/GaN interface: polarization Difference and conduction band discontinuity

formation of a triangular QW → 2D electron gaz (2DEG)

Electron density $N = \sigma / q$

Comparison of Si, GaAs and GaN

- **Comparison of the main properties for power and microwave applications**



https://sudonull.com/post/29796-Why-silicon-and-why-CMOS

Hetero-Epitaxial Growth of GaN on Si

- **Lack of GaN native substrates:**
  - limited supply & very expensive (few thousand $)

→ **Growth on Si (less than 100 $ for 200 mm wafer)**
--> large lattice-mismatch & thermal mismatch

Table 1
Material properties of GaN, AlN, Si, SiC, and sapphire (the given thermal expansion coefficient is an averaged value and might differ significantly at very low and at high temperatures) [7–9, 13–18]

material	a (Å)	c (Å)	thermal conductivity (W/cm K)	thermal expansion coefficient in-plane (10^{-6} K^{-1})	lattice mismatch GaN/substrate (%)	thermal mismatch GaN/substrate (%)
GaN	3.189	5.185	1.3	5.59	–	–
AlN	3.11	4.98	2.85	4.2	2.4	25
Si(111)	5.430	–	1–1.5	2.59	−16.9	54
6H-SiC	3.080	15.12	3.0–3.8	4.2	3.5	25
sapphire	4.758	12.991	0.5	7.5	16	−34

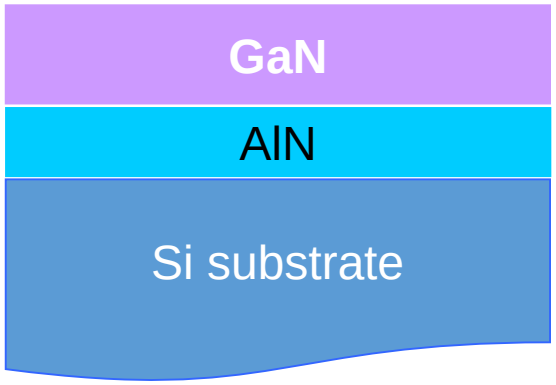
Hetero-Epitaxial Growth of GaN on Si

- **Main difficulties:**

- the "melt-back etching" --> reaction between Ga & Si at high temperature

If Ga comes into contact with Si during growth, this leads to melt-back etching which generates large defects in the GaN structures.

Use of a blocking layer between GaN and Si --> AlN



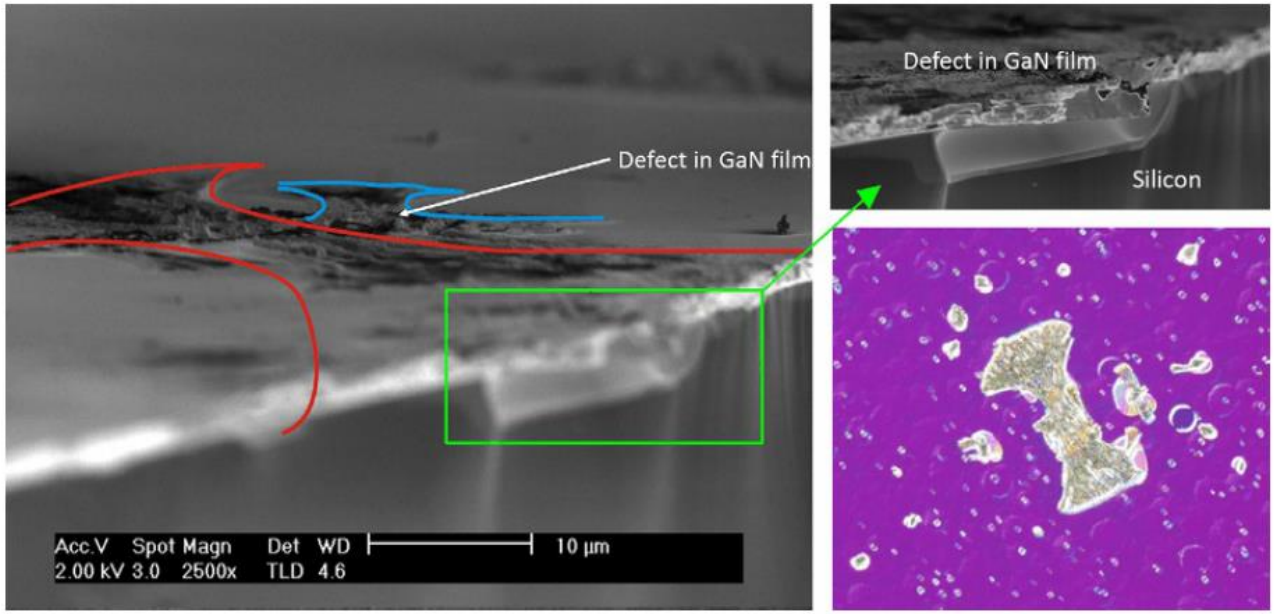
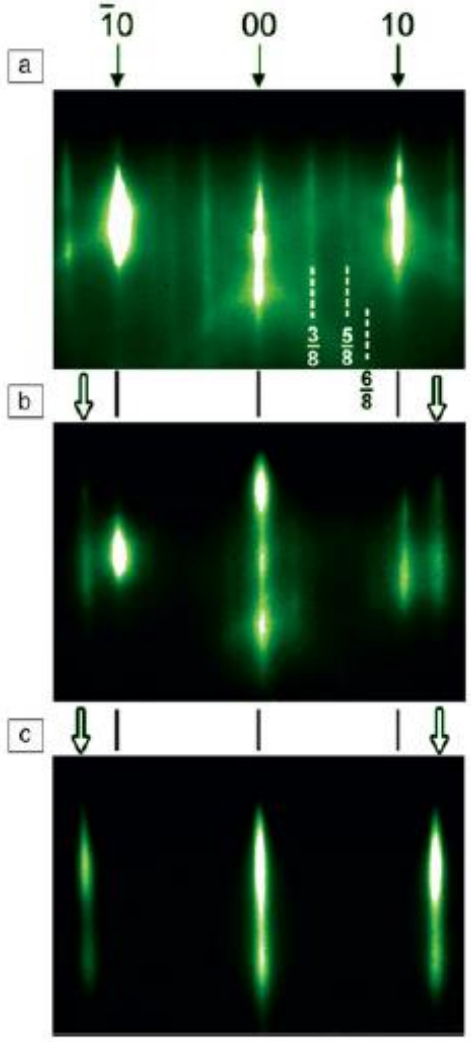


FIG. 4.2 Melt-back etching in silicon, with Nomarski image (bottom right), and etched hole in silicon as shown in the SEM images (left and top right). The *colored lines* show the outlines of the defects that are shown in the optical microscope image.

Chapter 4 – III-N Epitaxy on Si for Power Electronics
M. Charles, Y. Baines, E. Morvan and A. Torres
High Mobility Materials for CMOS Applications.
https://doi.org/10.1016/B978-0-08-102061-6.00004-5

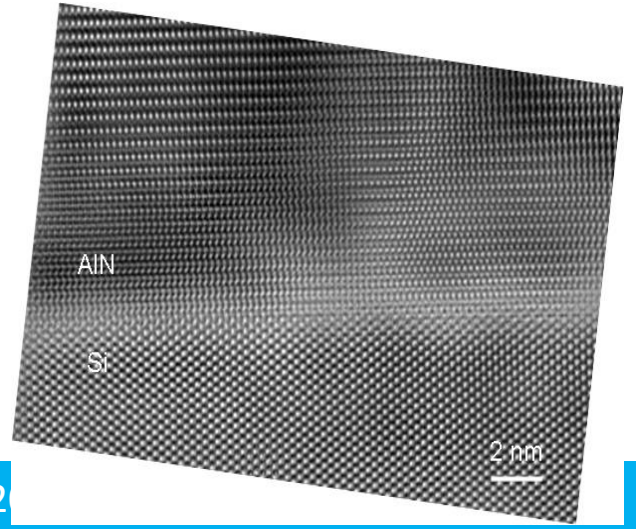
AlN Buffer Layer on Si by MBE

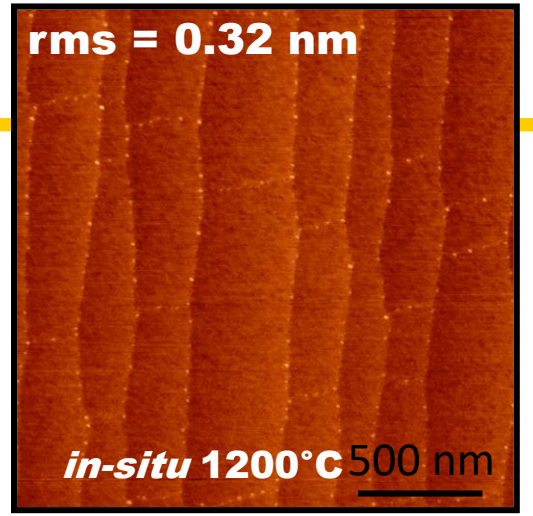
- **Nucleation process to obtain a sharp AlN/Si interface**

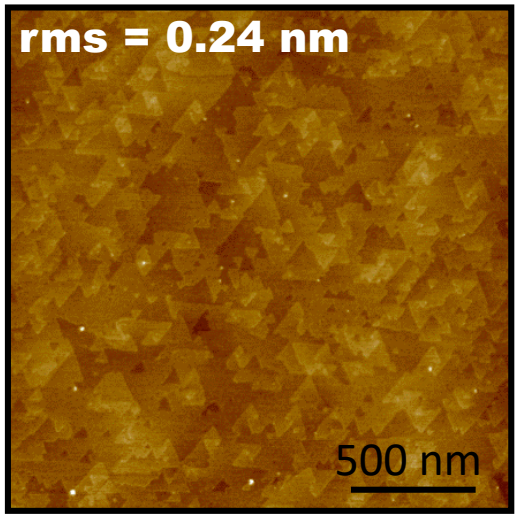


RHEED patterns along the [−110] azimuth of Si(111) during AlN nucleation using a NH_3-first nucleation process.
(a)after NH_3 pre-flow of Si(111) at 650°C and rapid thermal annealing at 820°C, a (8 × 8) surface Reconstruction characteristic of β -Si_3N_4 (0001) surface is obtained.
(b) After deposition of 1 monolayer of Al at 650°C, the AlN(0001) (1 × 1) orders indicated by white arrows Coexist with the Si(111) ones.
(c) after the growth of 40 nm AlN buffer layer at 920°C.

F. Semond , MRS BULLETIN
VOLUME 40, MAY 2015
DOI: 10.1557/mrs.2015.96







AFM

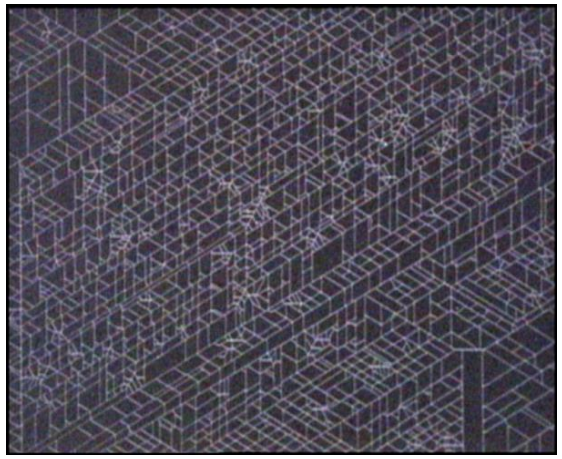
Hetero-Epitaxial Growth of GaN on Si

- **Main difficulties:**
  - **the melt-back etching --> reaction between Ga & Si at high temperature**
  - **high dislocation density --> high lattice-mismatch**
  - **large stress --> high thermal mismatch**

aGaN = 0.318 nm, $\alpha = 5.59 \times 10^{-6}\ K^{-1}$
aSi(111) = 0.384 nm, $\alpha = 3.59 \times 10^{-6}\ K^{-1}$
lattice-mismatch = 16.9%
TEC mismatch = 56%

Integration of GaN on silicon --> « manufacturability »
(compatibility of the wafers with a standard Si production line

Low bow, low particule/defect count of the wafers & crack-free surface



Cracking of a GaN/Si structure due to the large tensile stress during the cooling process from growth temperature to room temperature originating from the TEC mismatch

Design of the Heterostructure

- **Integration of layers to control the strain:**

To grow crack-free GaN layers on Si, it is necessary to maintain a certain amount of **compressive strain in GaN** in order to compensate for the tensile strain appearing during the post growth cooling from the growth temperature to room temperature.

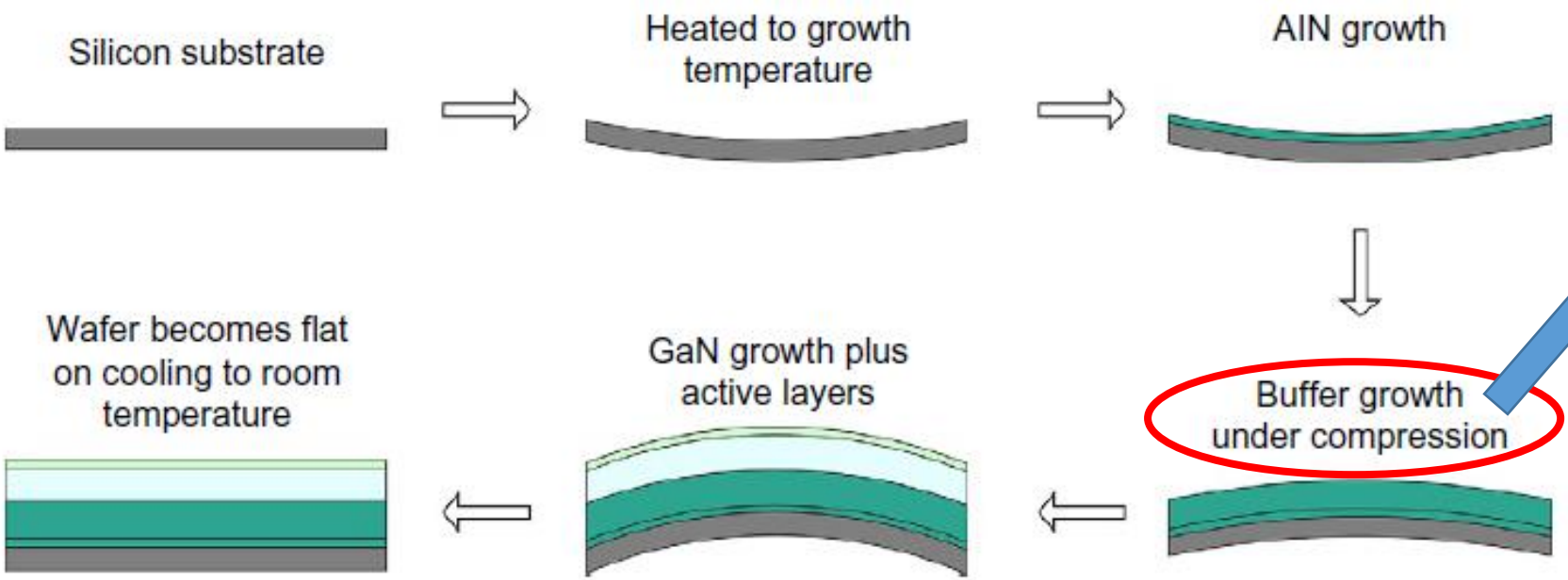


FIG. 4.4 Schematic of basic GaN-on-silicon growth.

Growth under compressive strain --> low Al content Layers on high Al content ones

to prevent cracking, **growth of GaN must be 2D**, which also means that **the surface morphology of the initial AlN or AlGaN buffer layer** needs to be as smooth as possible.

Design of the Heterostructure

➢ **Designing structures to preserve a compressive strain:**

1. Graded aluminum from AlN to GaN: with either a smooth grading or a step grading of different $Al_xGa_{1-x}N$ layers

➡ to continually introduce compression into the layers.

2. AlN interlayers: after growing GaN on the Al(Ga)N nucleation layer, a new AlN layer is grown on this GaN layer. The AlN quickly reaches its critical strain thickness and then relaxes. After, **a GaN layer is grown in compression** on the AlN layer.

➡ Presence of a strain gradient during the growth of the different layers (a slope of zero = fully relaxed structure)
Strong difference in the relaxation process between the first & second GaN layer → compressive strain of the structure

↪ **compensation of the tensile strain generated during the cooling process** (In-situ curvature measurement of the sample gives the average deformation of the epitaxial structure)

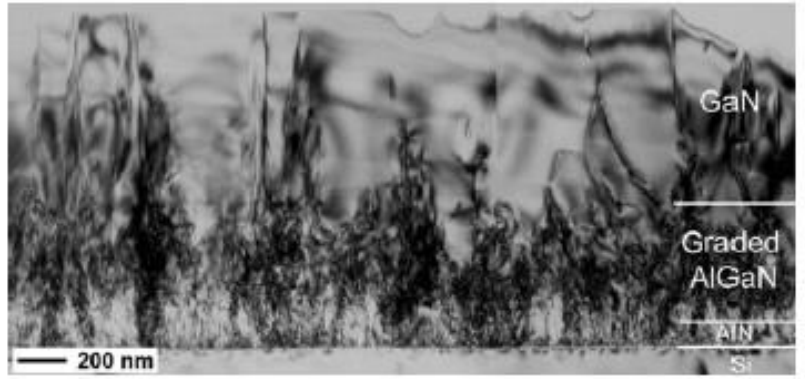
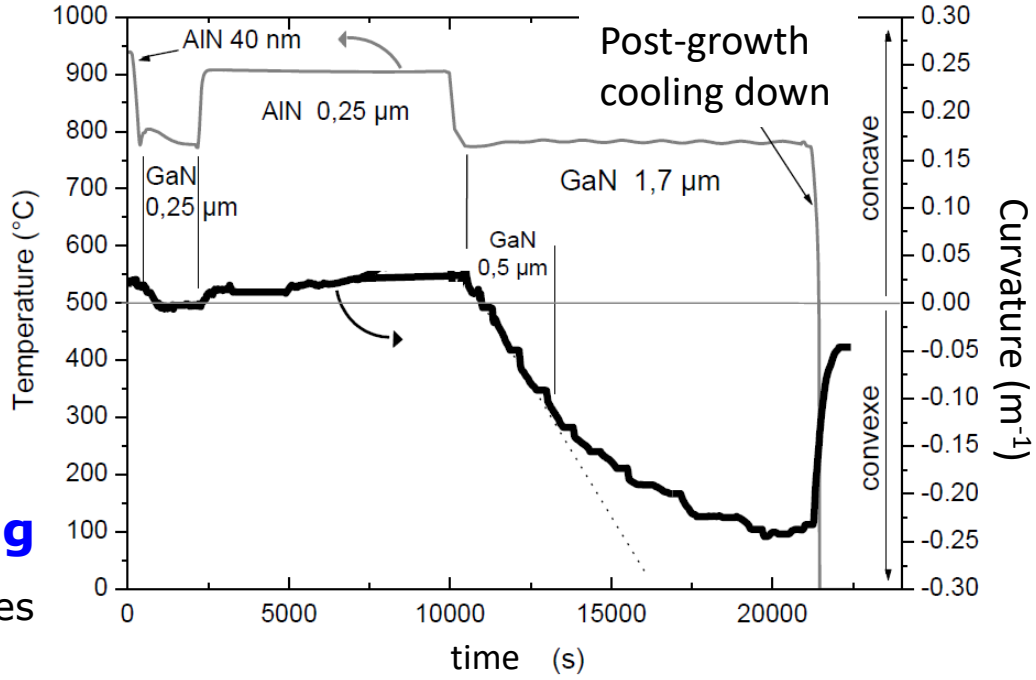


Fig. 7 Cross-sectional TEM image of GaN grown on the graded AlGaN buffer [39]

[B. Zhang et al., Chin. Sci. Bull. 1251 (2014)]



Effect of the Barrier Material

➢ **Designing structures to improve the HEMT characteristics:**

1. The AlGaN/AlN/GaN double heterojunction

with an AlN layer of ≈ 1nm between the AlGaN barrier & the GaN channel.

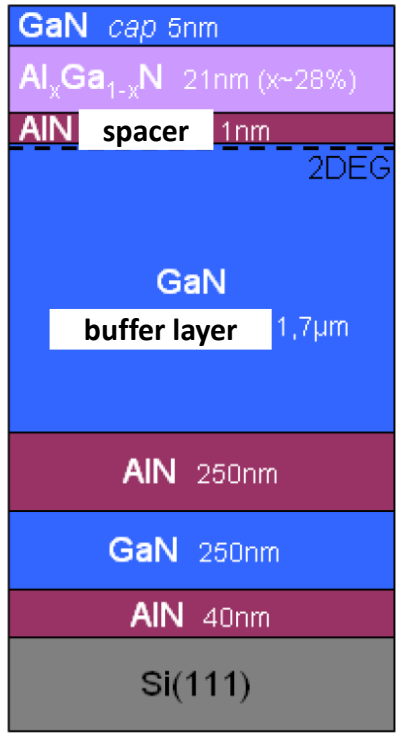
AlN "spacer" layer ⟹ maintains **high mobility at high sheet charge densities** by increasing the effective CB offset & decreasing alloy scattering.

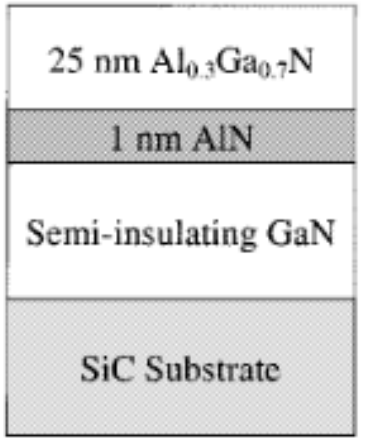
It allows more e- to accumulate in the GaN channel combined with better confinement due to the larger band offset which increases the mobility,

this gives lower sheet resistance:

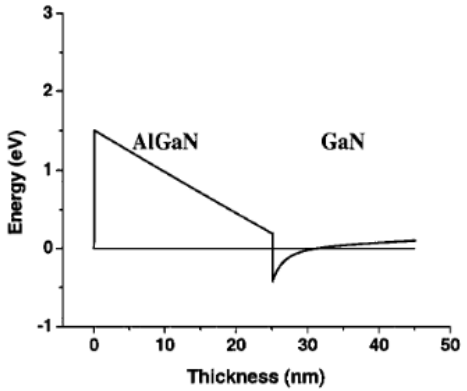
$$R_{sh} = \frac{1}{e\mu N_s}$$

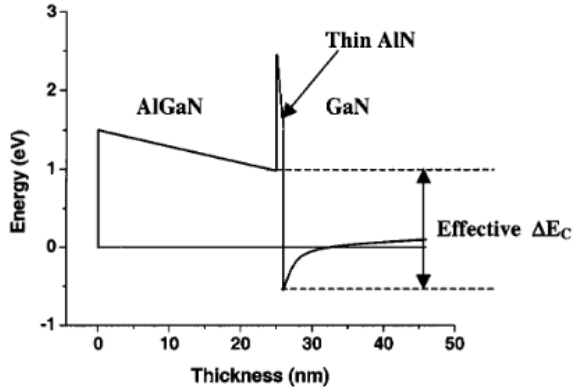
[N. BARON, thèse, Univ. Nice (2009)]





[L. Shen et al., IEEE EDL 22, 457 (2001)]





Schematic of a typical AlGaN/GaN HEMT structure

Effect of the Barrier Material

➢ **Designing structures to improve the HEMT characteristics:**

2. Design of the AlGaN capping with:

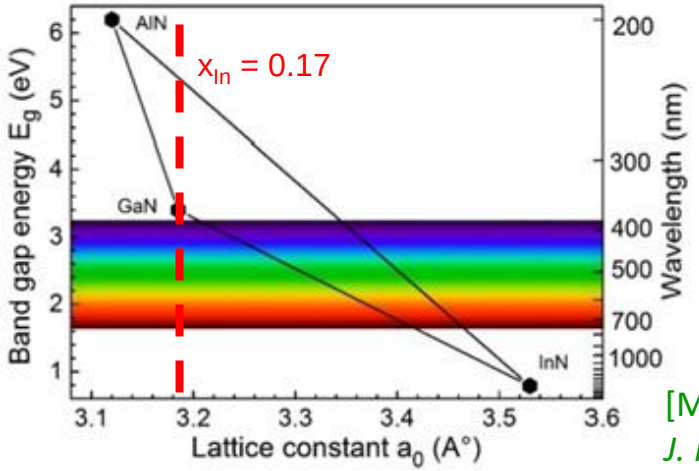
- larger Al content or

- lattice-matched alloys (InAlN, ScAlN)

to reach larger Ns values.

[S. RENNESSON, thèse, Univ. Nice (2013)]

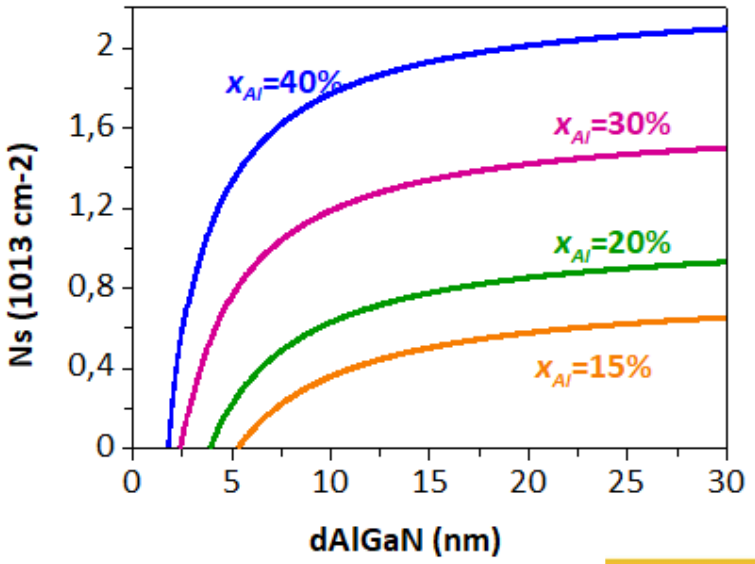
[Y. Cordier et al., III-Nitride Semiconductors & their Modern Devices (2013)]

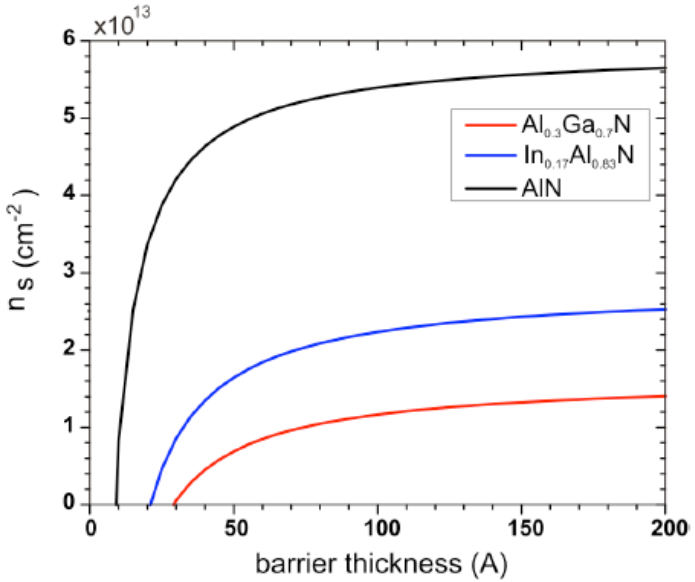


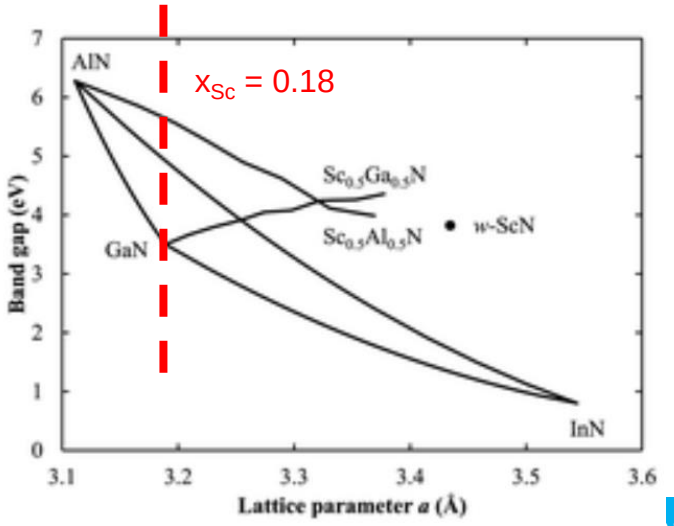
[M. A. Moram et al., *J. Mater. Chem. A*2, 6042 (2014)]

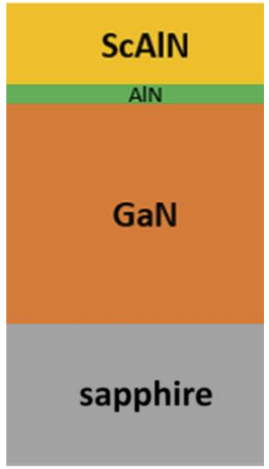
Mobility μ > 1800 $cm^2.V^{-1}.s^{-1}$

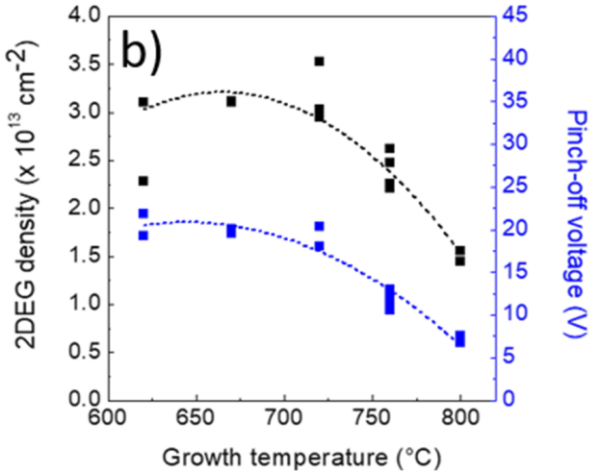
Sheet carrier density > 1x10^{13} cm^{-2} @ 300K











[C. ELIAS et al., APL *J. Mater. 11*, 031105 (2023)]

2D Materials

Van der Waals (2D) Materials

- **Graphene: an atomic-scale honeycomb structure made of carbon atoms**
  it is the thinnest two-dimensional material in the world
  obtained by mechanical exfoliation of graphite (tape)


© The Nobel Foundation. Photo: U. Montan
Andre Geim

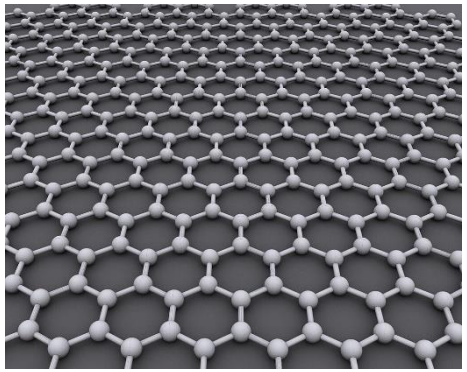

© The Nobel Foundation. Photo: U. Montan
Konstantin Novoselov

Nobel Prize in Physics (2010)

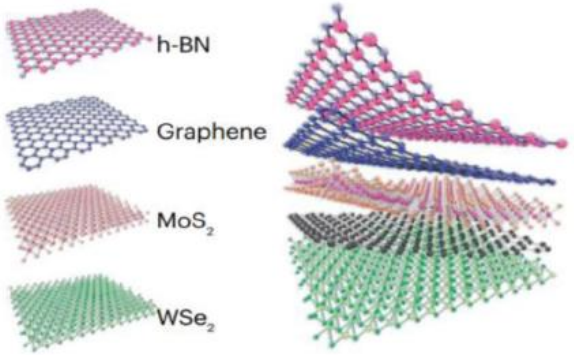
- Graphene shows exceptional properties in electronics and

In quatum physics: such as high mobility, tunable carrier concentration, the quantum Hall effect, tunable band gap and optical response, High thermal and chemical stability etc…

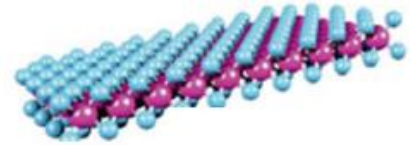
[https://en.wikipedia.org/wiki/Graphene#cite_note-nobel2013-52]

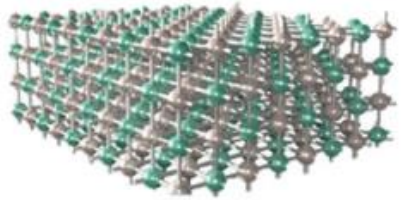


- **2D materials: layered structure with covalent bonds along the in-plane direction & weak van der Waals bonds along the out-of-plane direction**

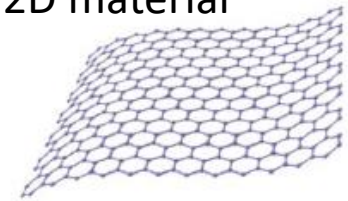



Bulk semiconductor


2D material



Rough surface, dangling bonds

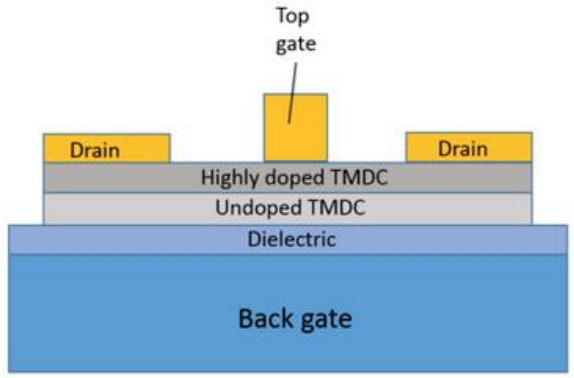


NO dangling bonds !

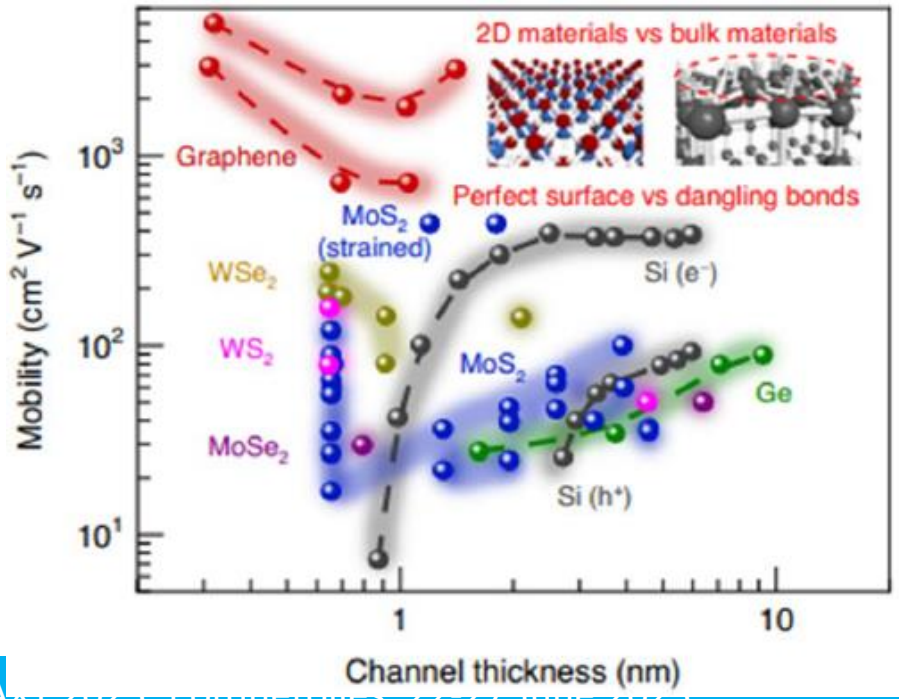
2D materials-based CMOS electronics

Synthesis of 2D Materials

- **The mechanical exfoliation of 2D materials using scotch tape gives high-quality flakes but of limited size (< mm), which cannot be used for the fabrication of devices.**
- **Large-area thin films of 2D materials with high crystalline quality and spatial uniformity are being investigated by CVD and MBE.**
- **Fabrication of various 2D materials including graphene, h-BN (hexagonal boron nitride), and TMDs (transition metal dichalcogenides, e.g. MoS_2, WSe_2 etc.).**
- **Using 2D material as the channel of a MOS-FET or HEMT with high-mobility performances for ultra-thin layers**



[https://en.wikipedia.org/wiki/Two-dimensional_semiconductor]



[Katiyar et al., Nano Convergence (2025) 12:11]

Van der Waals Epitaxy

- **Heteroepitaxy → band structure design & engineering for high performance devices**
- **Epitaxial stress:**

  $\varepsilon = (a_{sub.} - a_{lay.}) / a_{lay.}$

  → $\varepsilon < 0$: compressive stress

  → $\varepsilon > 0$: tensile stress

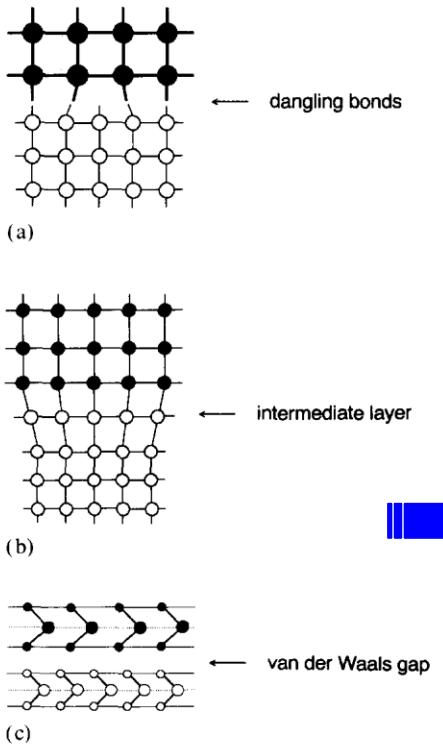


Fig. 1. Interfaces connected by (a) covalent bonds, and (c) a van der Waals gap.

Critical thickness (pseudomorphic growth)

$h_c \propto 1 / \varepsilon$

For $h > h_c$: strain relaxation (creation of defects)

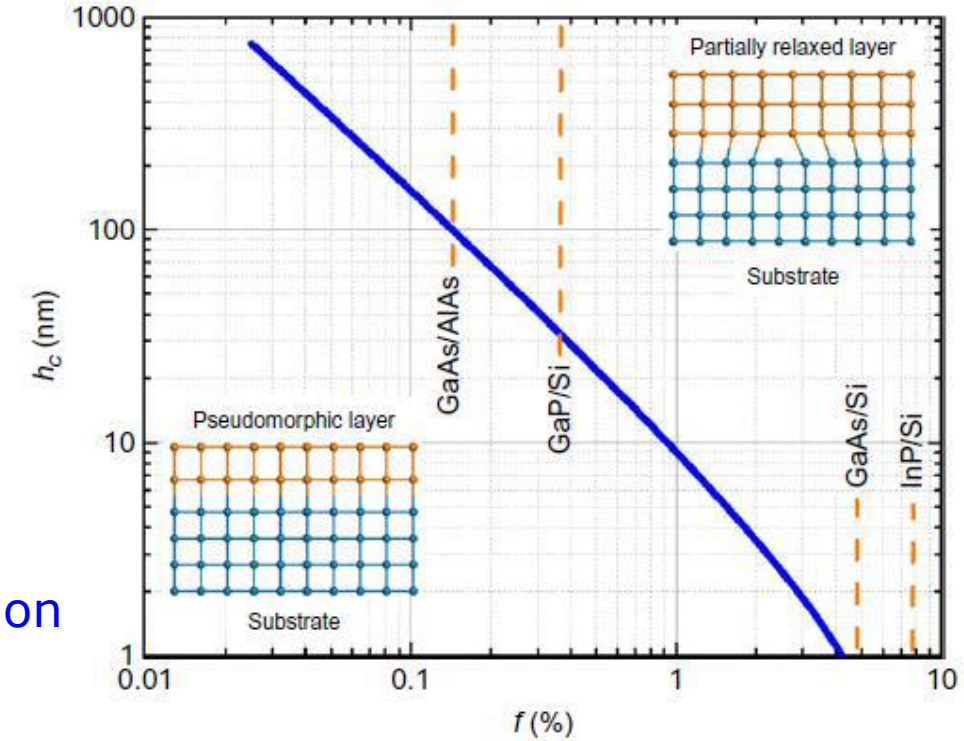


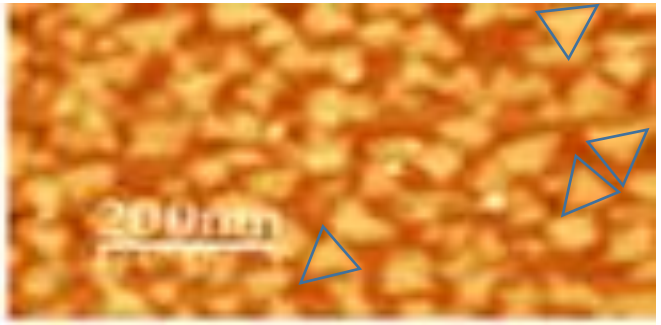
FIG. 3.3 Theoretical critical thickness h_c in function of lattice mismatch f.

Chapter 3 – Monolithic Integration of InGaAs on Si(001) Substrate for Logic Devices , Clément Merckling High Mobility Materials for CMOS Applications. https://doi.org/10.1016/B978-0-08-102061-6.00004-5

A 2D material has layers bound by van der Waals interactions (dist. dependent interaction). Surfaces are without dangling bonds. Its growth can be expected to induce very limited lattice distortion even for a large lattice-mismatch between the deposited film and the host substrate.

Synthesis by Thin Film Deposition

- **Target: a deposited 2D material with wafer-scale uniformity and minimal defects**



MoS_2 on GaN/sapphire by MBE
[M. Al Khafioui et al.,
J. Crystal Growth **652**, 128047 (2025)]

- **It is fundamental to control the kinetic of 2D materials:**
  - **non-uniform (random) nucleation,**
  - **formation of grain boundaries during coalescence**
  - **nucleation of another layer before reaching full surface coverage**

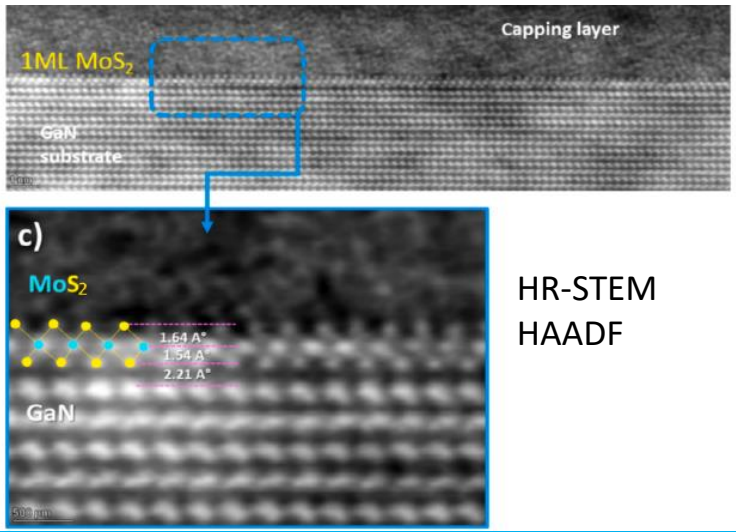
Need to find growth recipes to reach the full control of :

- **the nucleation process (nucleation sites);**
- **the deposited thickness at the monolayer level;**
- **the coalescence of the 2D islands.**

Investigation of MoS_2

- **Integration of MoS_2 on GaN on sapphire**
- **Advantages of MBE:**
  - **precise control over deposition;**
  - **ultra-pure elements;**
  - **in-situ monitoring of growth by RHEED;**
- **MoS_2 has a similar lattice parameter & thermal expansion coef. vs. GaN ($\varepsilon \approx 1\%$)**

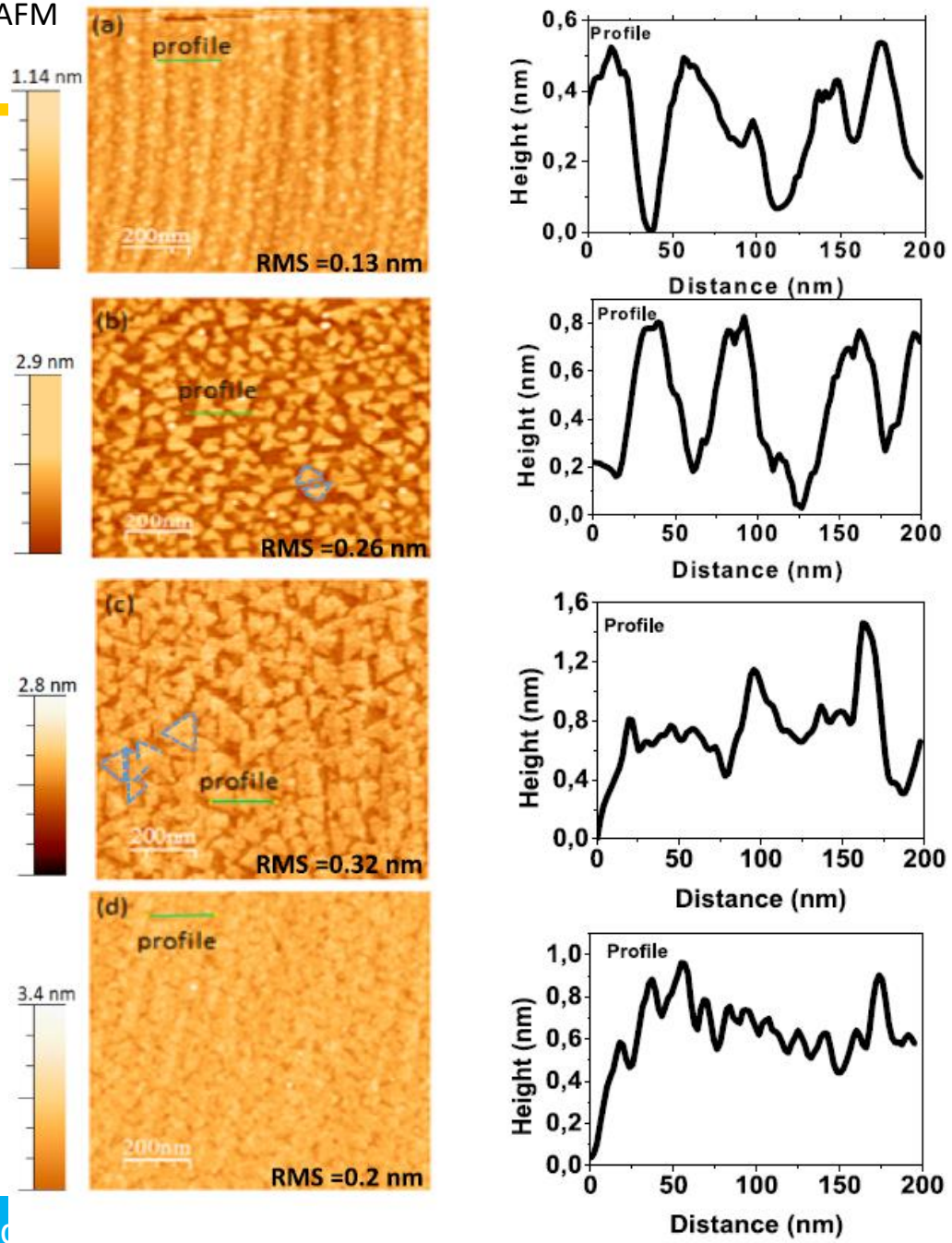
➡ **Control of the surface morphology of MoS_2 from islands nucleation step until a full surface coverage** (with growth times of 30 min., 1h, 2h, 3h from (a) to (d))



HR-STEM
HAADF

[M. Al Khafioui et al., J. Crystal Growth **652**, 128047 (2025)]

AFM



Investigation of MoS_2

- **Growth of wafer-scale MoS_2 monolayer on sapphire (industry-compatible substrate)**
- **Use of low-pressure CVD**
- **Importance of the epitaxial relationship :**

Engineering of the surface orientation & preparation:

- Design of the miscut angle orientation

- Ordering of the triangular MoS_2 domains

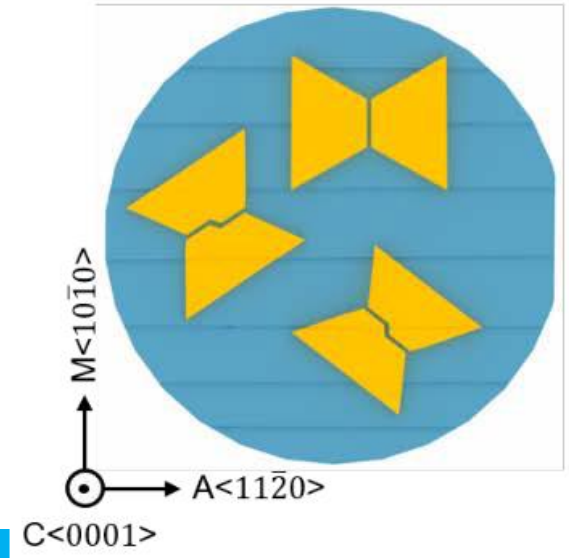
[T. Li et al., Nature Nanotechnology **16**, 1201 (2021)]

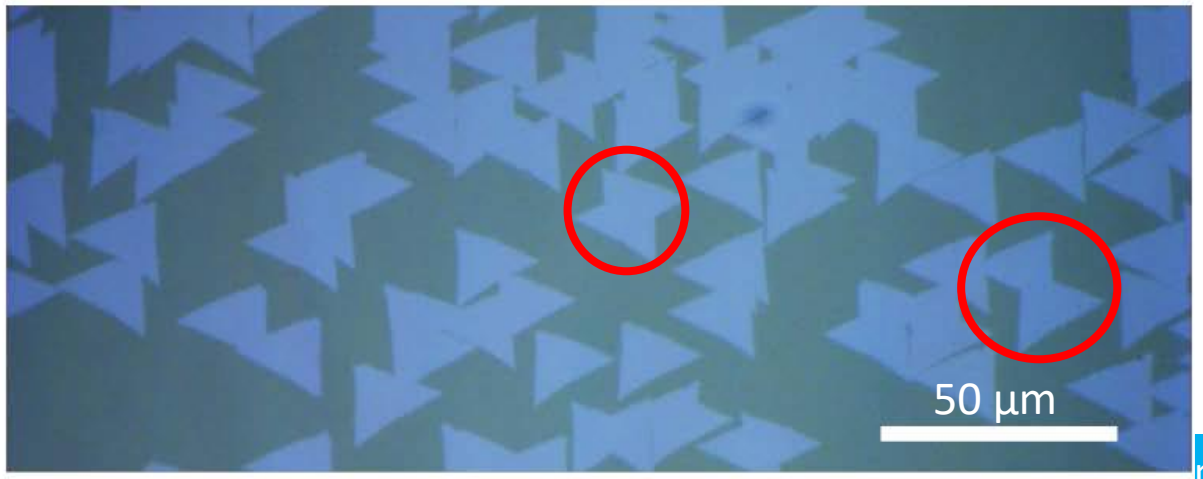
Standard C-plane sapphire substrates have a miscut angle towards M axis

However, one edge of the triangular domains is perpendicular to A axis

The growth of the two antiparallel domains is possible

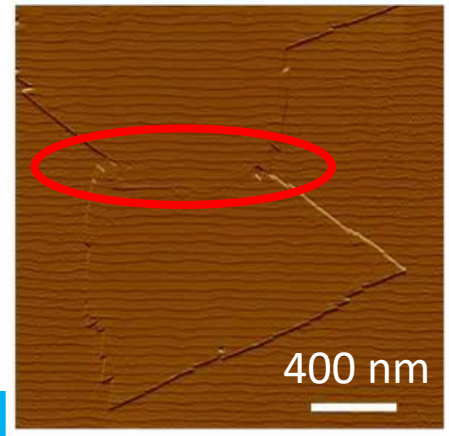
Prevents the growth of a single crystal !





Optical image

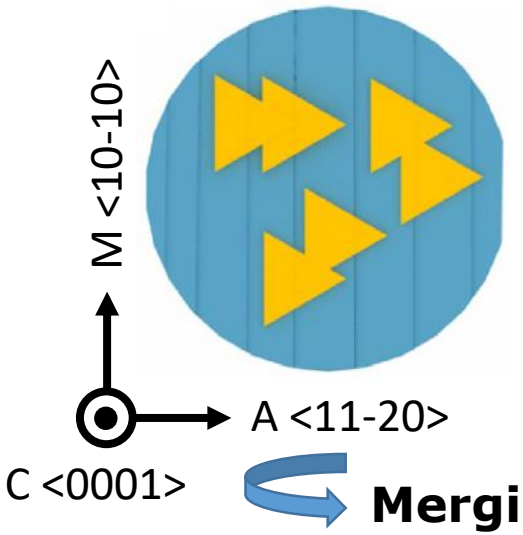
AFM Amplitude

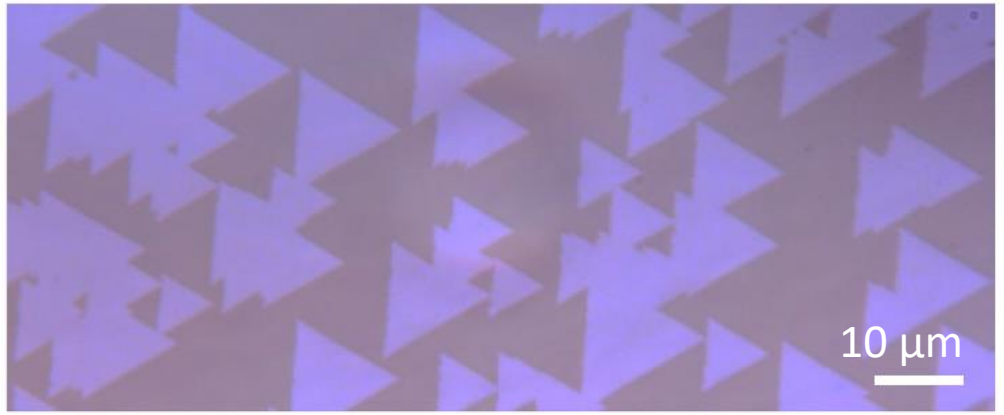


Wafer-scale MoS_2 on 2-inch sapphire

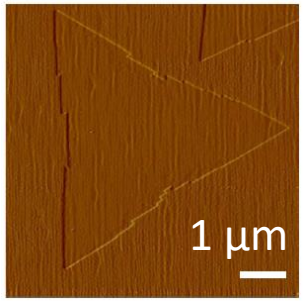
- **Design of c-plane substrates with a miscut angle towards the A-axis to prevent the formation of antiparallel MoS_2 domains**

➡ **This surface terrace/step geometry enables the growth of MoS2 triangular domains with > 99% unidirectionnal alignment on 2-inch wafer !**

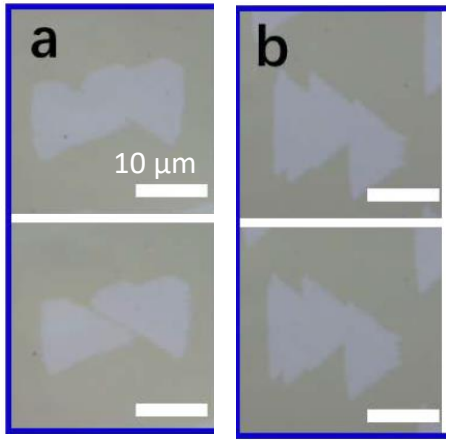




Optical image



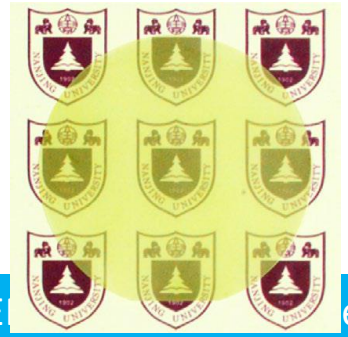
AFM Amplitude

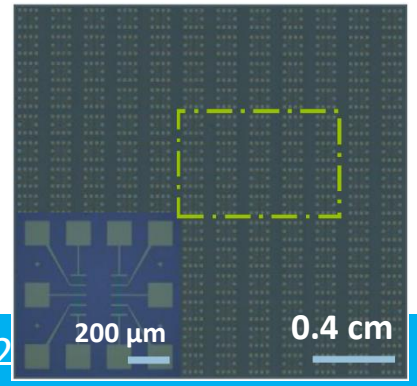


Merging of the unidirectional domains is obtained without the formation of grain boundaries (etching = grain boundaries)

➡ **Wafer-scale MoS_2 single crystals & fabrication of FETs**

[T. Li et al., Nature Nanotechnology 16, 1201 (2021)]





Challenges to overcome

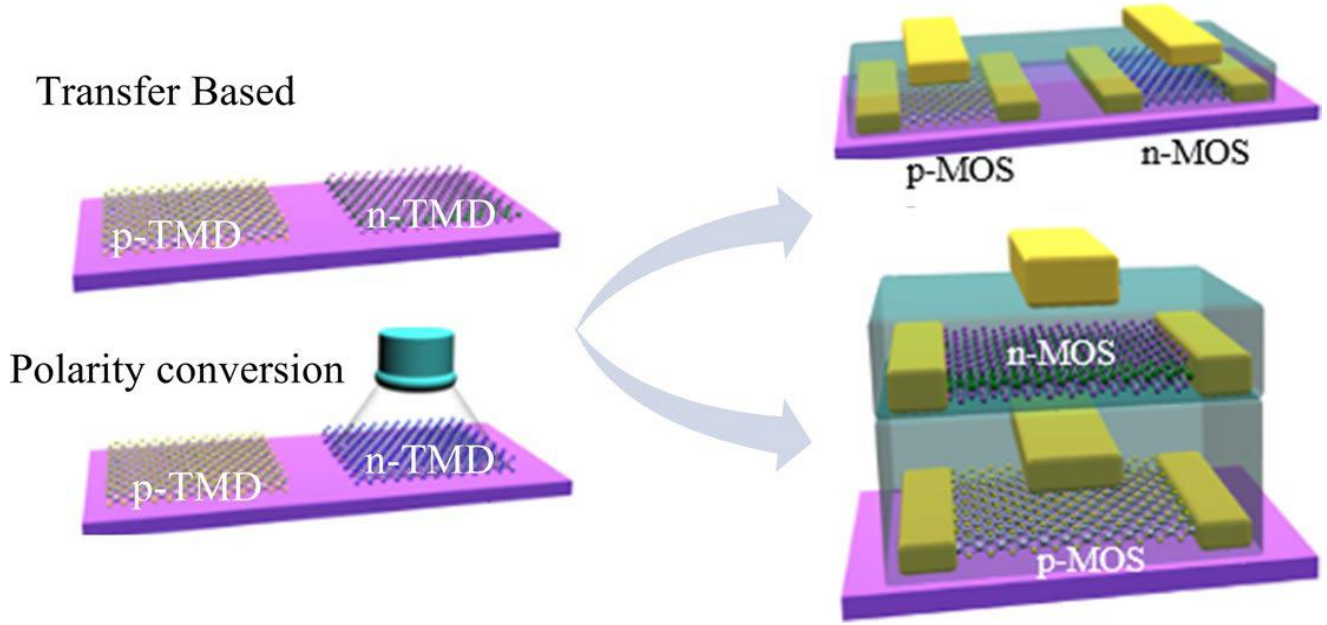
- **2D materials still face several limitations that impede their use for CMOS-compatible synthesis such as :**

  - High contact resistance

  - Deposition of high quality dielectric materials

  - Selective doping for local p- or n-type conversion

  - High thermal budget process for large area / defect-free materials



[Katiyar et al. Nano Convergence (2025) **12**:11 https://doi.org/10.1186/s40580-025-00478-1]

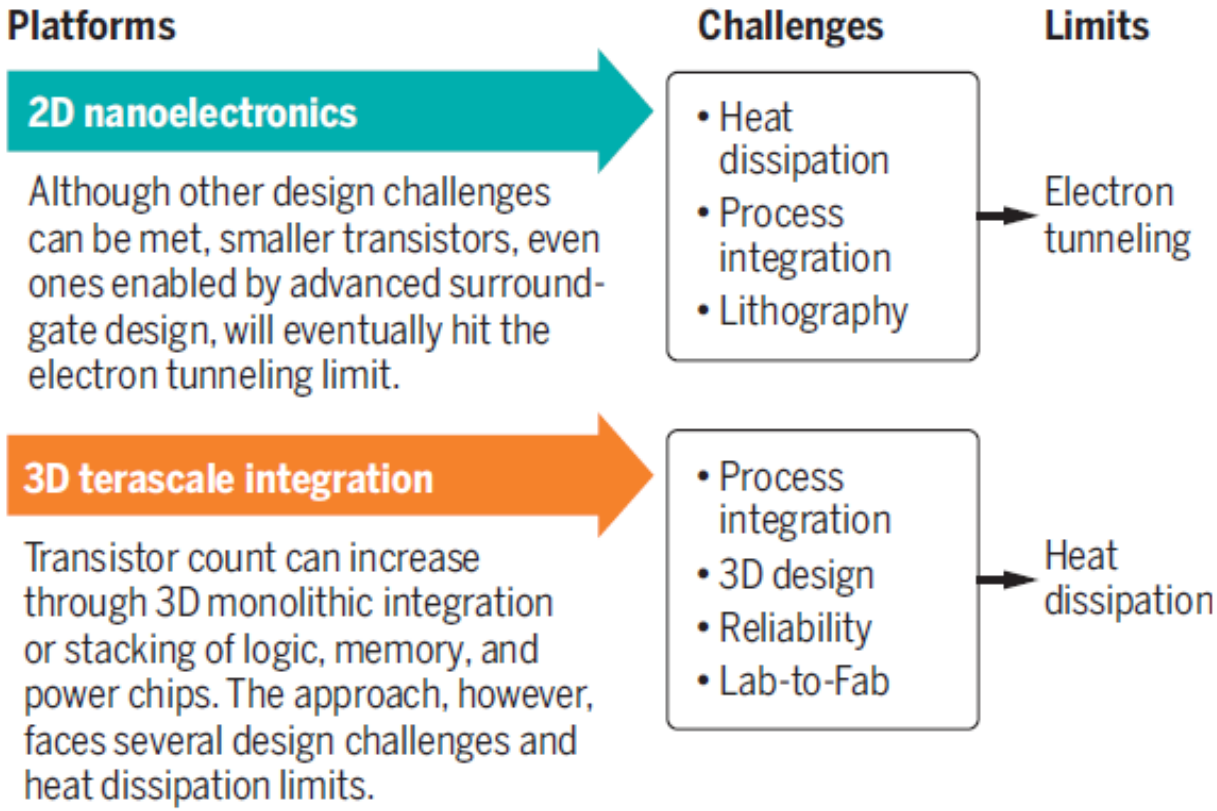
Conclusions & Perspectives

Conclusions

- **Since the first integrated circuit, the microelectronics industry has completely revolutionized our society and our lifestyles.**
- **Combining material engineering (hetero-integration, strain), device architecture, miniaturization & density, the performances of devices are still reaching new standards at a very high rhythm.**
- **Fabrication platforms include:**
  - **2D Nanoelectronics**
  - **3D Architectures**

Fundamental Limits due to Tunneling effects & Heat generation

[Mark S. Lundstrom et al., Science **378**, 722 (2022)]

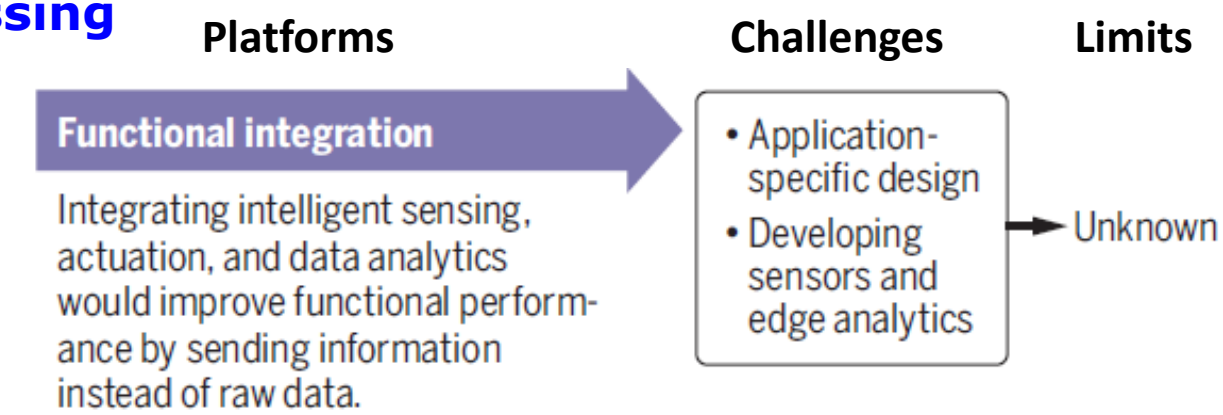


Perspectives

- **Development of chips that accelerate specific functions ("specialized" chips or ICs)**
  --> increasing the rate of information processing

Compagnies designing their own chips

[Mark S. Lundstrom et al., Science 378, 722 (2022)]



- **Specific-design chips :**
  high cost (up to 500 M$)
  team of 1000 engineers

- **Limits :**
  Technology cost --> 20 B$ for a leading-edge fab ... (vs. 1 B$ in 2000)
  Environmental footprint ?

*"**Sustainability is becoming a key component of business and regulations** due to concerns on climate change, resource depletion and pollution. **The IC manufacturing is resource** intensive and due to the increase in complexity from node to node we find **the number of process steps increase by 2.6x and the resulting associated energy need by 3.5x when scaling from iN28 to iN3**. Simultaneously the greenhouse gas emissions and water usage are increasing accordingly. Prompt actions are needed from the industry to mitigate these effects".*

[L-Å Ragnarsson et al., IEEE (EDTM) (2022) - 10.1109/EDTM53872.2022.9798208]

Special thanks to my colleague
Prof. Mohamed AL KHALFIOUI

Thank you for your attention !